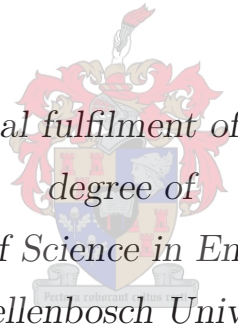
Investigation into a Proposed HVDC Series Tap Topology

by

André Hartshorne



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Abstract

HVDC Transmission has found widespread application through-out the world. The typical HVDC Transmission system consists of two terminals and provides point-to-point large scale power delivery. HVDC Transmission systems can be extended to become multi-terminal systems. Introducing series taps is the easiest way to achieve this.

Introducing a HVDC Series Tap into a HVDC Transmission system presents several challenges. These include the additional voltage drop present on the line, switching noise introduced by the use of a power electronic converter and providing galvanic isolation between the line potential and the ground potential. Several topologies have been proposed but none has been accepted as the industry standard implementation.

This thesis discusses the design of a HVDC Series Tap utilising an air-core transformer. A scale model of the proposed HVDC Series Tap is constructed and implemented on a HVDC Transmission Line model. Experimental results are presented.

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Uittreksel

Hoogspanning Gelykstroom Transmissie word tans wêreldwyd toegepas. Die algemene Hoogspanning Gelykstroom Transmissiestelsel bestaan uit twee terminale en word gebruik om drywing van punt tot punt te verskaf. Hoogspanning Gelykstroom Transmissiestesels kan uitgebrei word om uit meer as twee terminale te bestaan. Die eenvoudigste manier om hierdie doel te bereik is om serie aftap punte by te voeg.

Om 'n Hoogspanning Gelykstroom Serie Tap tot 'n Hoogspanning Gelykstroom Transmissiestelsel by te voeg bied verskeie uitdagings. Hierdie uitdagings sluit die teenwoordigheid van 'n addisionele spanningsval oor die lyn, skakelruis wat weens die gebruik van skakelelektronika ontstaan en die voorsiening van galvaniese isolasie tussen die lynpotensiaal en grondpotensiaal in. Verskeie topologieë is al voorheen voorgestel, maar geen word aanvaar as die industrie standaard nie.

Hierdie tesis bespreek die ontwerp van 'n Hoogspanning Gelykstroom Serie Tap wat van 'n lugkerntransformator gebruik maak. 'n Model op skaal is van die voorgestelde Hoogspanning Gelykstroom Serie Tap gebou en op 'n model van 'n Hoogspanning Gelykstroom Transmissiestelsel geïmplementeer. Eksperimentele resultate word voorgelê.

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Contents

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Nomenclature

Abbreviations & Acronyms

AC	Alternating Current
DC	Direct Current
GTO	Gate Turn-off Thyristor
GW	Gigawatt
HV	High Voltage
HVDC	High Voltage Direct Current
IC	Integrated Circuit
IGBT	Insulated Gate Bipolar Transistor
kV	Kilovolt
LC	Inductor-capacitor
MOSFET	Metal-oxide-semiconductor Field-effect Transistor
MTDC	Multi-terminal High Voltage Direct Current
MW	Megawatt
PI	Proportional-Integral
PWM	Pulse Width Modulation
RC	Resistor-capacitor
RMS	Root Mean Square

Variables & Constants

α	Fire angle of a thyristor bridge
α_i	Fire angle of a thyristor inverter

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α_r	Fire angle of a thyristor rectifier
β	Angle of advance of a thyristor inverter
γ	Extinction angle of a thyristor inverter
θ_{c-s}	Thermal resistance between the case of the component and the heat sink
θ_{j-c}	Thermal resistance between the junction and the case of a component
θ_{s-a}	Thermal resistance between the heat sink and surrounding air
μ_0	Permeability of free space
τ	Time constant of a resistor-capacitor circuit
Φ	Magnetic flux
ω	Frequency in radians
B	Magnetic flux density
B_m	Magnetisation current parameter of the equivalent transformer model
C_{snub}	Snubber capacitor
D	Duty cycle of a converter
$D(s)$	Transfer function of a controller
d	Distance between two electrodes
f	Frequency of the voltages that supplies thyristor converters
f_{BW}	Bandwidth of the designed controller
f_s	Switching frequency of a converter
$G(s)$	Transfer function of the plant to be controlled
G_c	Core loss parameter of the equivalent transformer model
h_{AC}	Order of the harmonics present of the AC-side of a thyristor converter
h_{DC}	Order of the harmonics present of the DC-side of a thyristor converter
I_{TM}	Peak on-state current of a thyristor
h_{pri}	Height of the primary winding of an air-core transformer
h_{sec}	Height of the secondary winding of an air-core transformer
I_{1rated}	Rated current of the primary winding of the transformer being tested
I_d	Load current of a thyristor converter bridge

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I_{line}	The current flowing between terminals of a HVDC transmission system
I_{load}	The current that flows through the load resistance of a HVDC series tap
I_{model}	Output current of the HVDC Series Tap model
I_{ref}	The current that must flow between the terminals of a HVDC transmission system
k	Coupling factor of mutually coupled inductors
k_i	Gain of the integral term of a PI-controller
k_p	Gain of the proportional term of a PI-controller
L	Inductance
L_{eq}	Series inductance of a transformer being tested
L_s	Supply inductance of a thyristor converter bridge
L_{series}	Total supply inductance used for the snubber calculation
$\bar{l}$	Length of a vector
M	Mutual inductance of an air-core transformer
N	Negative terminal of a HVDC Transmission Line model
P	Positive terminal of a HVDC Transmission Line model
P_1	The real power delivered through the primary winding to the transformer being tested
P_{loss}	Power loss of a component
P_{model}	The power delivered by the HVDC Series Tap model
P_{ref}	The amount of power to be transmitted by a HVDC transmission system
p	Pressure of a gas
p_n	Pulse number of a thyristor converter
p_{pri}	Pitch of the primary winding of an air-core transformer
p_{sec}	Pitch of the secondary winding of an air-core transformer
Q_{rr}	Recovered charge when a thyristor
$\bar{R}$	Vector from source point to field point
R_{ci}	Commutation resistance of a thyristor inverter

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R_{cr}	Commutation resistance of a thyristor rectifier
R_{eq}	Copper resistance of the equivalent transformer model
R_{line}	Resistance of a HVDC transmission line
R_{load}	The load resistance connected to HVDC series tap
R_{model}	The load resistance connected to the HVDC Series Tap model
R_{on}	The on-resistance of a MOSFET
R_{snub}	Snubber resistance
r_{pri}	Radius of the primary winding of an air-core transformer
r_{sec}	Radius of the secondary winding of an air-core transformer
S_{rated}	The total rated power of the transformer being tested
s	Integration surface
T	Switching period
T_{amp}	Ambient temperature
T_j	Junction temperature
T_{off}	Rise time of a MOSFET
T_{on}	Rise time of a MOSFET
V_{1rated}	The rated voltage of the primary winding of the transformer being tested
V_{1test}	The voltage applied to the primary winding of the transformer being tested
V_{ACinv}	The AC voltage across the AC-side of a thyristor inverter of a HVDC transmission system
V_{ACrec}	The AC voltage across the AC-side of a thyristor rectifier of a HVDC transmission system
V_B	Break down voltage of a substance
V_{bus}	Intermediate bus voltage used in series tapping configurations
V_{DCinv}	The DC voltage across the DC-side of a thyristor inverter of a HVDC transmission system
V_{DCrec}	The DC voltage across the DC-side of a thyristor rectifier of a HVDC transmission system
V_a, V_b, V_c, V_d, V_e & V_f	Supply voltages used for thyristor bridge design

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$V_{forward}$	The forward of a diode
$V_{inverter}$	Average input voltage of a thyristor inverter
V_{LL}	Line-to-line supply voltage of a rectifier- or inverter bridge
V_{load}	The voltage of a HVDC series tap that appears across the load
V_{model}	Output voltage of the HVDC Series Tap model
$V_{rectifier}$	Average output voltage of a thyristor rectifier
V_{tap}	The voltage that appears across a HVDC series tap
V_{th}	The voltage that appears across a thyristor
V_v	Maximum terminal voltage of a thyristor used in the snubber calculation
u	Commutation angle of a thyristor converter
X_{ci}	Leakage reactance of the transformers connected to a thyristor inverter
X_{cr}	Leakage reactance of the transformers connected to a thyristor rectifier
X_{eq}	Leakage reactance of the equivalent transformer model
Z_{eq}	Series impedance of the transformer being tested

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List of Figures

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Stellenbosch University https://scholar.sun.ac.za

Stellenbosch University https://scholar.sun.ac.za

Stellenbosch University https://scholar.sun.ac.za

List of Tables

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Chapter 1

Introduction

1.1 Background

High Voltage Direct Current (HVDC) concerns the transmission of bulk quantities of power through the use of DC voltages instead of AC voltages. Although HVDC transmission lines are less common than their AC counterparts, HVDC transmission serves a unique purpose. HVDC has additional applications that concern the inter-connection of asynchronous power networks, undersea power transmission and the stabilisation of large interconnected AC power systems.

Around 1929 Dr Uno Lamm developed a device that could rectify AC at high voltage levels. In the years following much research was done on HVDC and many accomplishments were made [4]. In 1954 the first commercially successful HVDC transmission line was completed. The system operated at a voltage of 100 kV and delivered 20 MW to the island of Gotland from the Swedish mainland [4]. Since the first HVDC system was constructed, many major HVDC systems had been constructed around the world. Today the total capacity of HVDC systems exceeds 75 GW [5].

The main advantage of a DC line is that it tends to be more economical when longer transmission lines are required. Similarly, AC lines tends to be more economical for shorter lengths. The costs of a transmission line includes the number of conductors, the need for compensation and terminal equipment.

A DC transmission line only requires two conductors whereas a three phase AC transmission line would require three conductors, which makes a DC line more economical than an AC line. Therefore, a DC transmission line better utilises the Right of Way granted for the transmission line construction. Furthermore, an AC line requires reactive power compensation all along the line. In contrast, a DC line requires no compensation, which also makes a DC line more economical. Lastly, a DC line requires high voltage converters and filters at the terminals of the line. An AC line does not require such costly equipment, which makes an AC line more economical for shorter distances. There is a length where a DC and an AC line would cost the

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same to set-up. This is referred to as the break even distance. Depending on the per unit price of the conductors, the break-even distance vary between 400 km to 700 km [6].

HVDC Transmission systems that is used for long distance power transmission typically consists of only two terminals. These systems are also described as point-to-point power delivery systems. A rectifier serves as the sending end, rectifying the generated power and feeding the HVDC transmission line. An inverter serves as the receiving end, introducing the power from the HVDC transmission line into the target AC power system [5].

Introducing additional terminals to a HVDC transmission line is not as simple as with an AC transmission line. A multi-terminal HVDC transmission line requires complex control schemes and fast communication between the terminals, making the addition of another terminal a challenging matter [5].

HVDC transmission schemes that have more than two terminals are referred to as multi-terminal HVDC transmission schemes. Publications on multi-terminal HVDC transmission date back to as early as 1963 [7]. Currently there are only two operational multi-terminal HVDC transmission schemes in the world. They are found in Corsica [8] and Canada [5].

The simplest way to extend a HVDC Transmission system to a multi-terminal system is to add tappings [5]. Adding a tap to the HVDC transmission line would create an additional terminal on the line, therefore creating a multi-terminal HVDC transmission scheme. A tap could be connected in series or parallel to the HVDC Transmission Line. Series taps are typically associated with lower power ratings [9]. Parallel taps are associated with higher power ratings. Taps of different connections can be included on the same system. Such a system is referred to as a hybrid system and have been simulated in [10].

Several tapping topologies have been proposed, but none of them have been accepted as the industry standard. According to [11], a series tap should have minimum construction and operational costs, not reduce the reliability of the HVDC Transmission system, the presence of the tap should not interfere with the operation of the terminal controls of the HVDC transmission system and the controls of the tap must be self-contained and The latter eliminates the need for fast communications required to coordinate the other terminals. These requirements the simplifies the implementation and the operation of a series tap.

A series tapping scheme using a 12-pulse thyristor bridge is proposed in [9]. The commutation voltages required for the thyristor bridge is provided by an AC generator driven by a DC machine that is connected to the line.

In [12], a series tap based on forced commutated converter technology is proposed. Simulations of the proposed tap were successful. It was found that the tap was not as sensitive to AC disturbances because of the forced commutated converter technology.

Another force commutated converter series tap is proposed in [13]. This series tap used three power converter stages to tap power from the DC line and deliver it to a local AC network.

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The topology consisted of three different stages. Therefore tap losses increased slightly.

In [11], the use of an air-core transformer to provide galvanic isolation is proposed. Further research is performed in [14], [15], and [16] and a topology is proposed. A digital simulation is used to confirm the operation of the topology. The results showed that 1 MW of power could be delivered.

In [17], a 25 MW soft-switched series tap for a ±500 kV HVDC Transmission line is proposed. The scheme consisted of minimal number of components including an air-core transformer to provide isolation. The simulation result shows that the tap functions well and responds well to disturbances.

There are several challenges to be overcome when a series tap is introduced to a HVDC Transmission system. The first concern is the additional voltage drop present on the line. This voltage drop will have an influence on the control of the HVDC Transmission system. Should the converter stations not be able to provide the required additional voltage, the HVDC transmission system will not be able to deliver the required amount of the power and the system might even become unstable.

Another challenge is how galvanic isolation is achieved between the line potential and ground potential. In several previously proposed taps, conventional power transformers are used. This thesis explores magnetic-, mechanical- and chemical energy transfer as possible solutions.

Additional noise is introduced to the line because of the switching action of the converter. Such noise may disrupt other systems already present on the line, like protection or communication systems.

The Cahora-Bassa system is currently the only HVDC Transmission line in South Africa and, because of the local context, is selected as a case study for the thesis. At full capacity, the Cahora-Bassa system delivers 1 920 MW to the South African Power Grid. The line originates in Mozambique and ends 1 414 km away in South Africa. The line voltage of the system is ±522 kV and operates at 1 800 A.

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1.2 Thesis Objectives

The objective of this thesis is to provide proof of concept for a commercially implementable series HVDC tap. For the purpose of this thesis, the tap must be able to deliver 2 MW in simulation. The following objectives are set to achieve this goal:

- The first objective of this thesis is to investigate the theoretical basis of HVDC Transmission. This will be achieved by conducting a thorough literature study. The Cahora-Bassa system will be used as a case study and will also be studied.
- A model of a HVDC Transmission Line will be constructed to gain insight into the workings of an HVDC Transmission Line. It will also serve as a platform to test the chosen series tap topology. The HVDC Transmission Line Model will have basic controllers implemented. The main focus of the thesis is not, however, the controllers, therefore sophisticated controller implementation is beyond the scope of this thesis.
- Several series tap topologies will be investigated. The different topologies will be compared in terms of efficiency, switch utilisation, number of switches required and the complexity of the topology. Two topologies will be chosen for further study.
- A simulation to determine the self-inductances, mutual inductance and coupling factor of an air-core transformer will be developed.
- A model will be built of the series tap topology that shows the most promise. The design equations will be derived and a model of the proposed topology will be constructed to serve as a proof of concept. Practical results will be presented.

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1.3 Thesis Outline

Chapter 2 presents literature topics that form the theoretical basis of this thesis. These topics include the different configurations used in HVDC Transmission, different types of converters used, HVDC control and previously proposed series tap topologies. The Cahora-Bassa HVDC Transmission system is also discussed.

Chapter 3 discusses the system level design and presents a system level simulation. Also discussed is the design of the hardware used to implement the HVDC Transmission Line Model. The open-loop operation of the HVDC Transmission Line Model is shown.

Chapter 4 covers the design, simulation and implementation of the thyristor converters used in the HVDC Transmission Line Model.

Chapter 5 presents the different topologies investigated for implementation. The chapter concludes with a comparison of the different tapping options.

Chapter 6 covers the analysis and simulation of an air-core transformer. The numerical method used to determine the self-inductances, mutual inductance and coupling factor is discussed. The chapter concludes with two methods to increase the coupling factor of the air-core transformer.

Chapter 7 analyses the first HVDC Series topology considered for construction. A simulation is performed to investigate the working of the converter. The chapter discusses the analysis of the this topology.

Chapter 8 analyses the second HVDC Series topology considered for construction. The design equations are derived for this topology. Simulation results of the topology is presented.

Chapter 9 holds the topology of the previous chapter implemented in practice to be integrated with the HVDC Transmission Line Model. The chapter discusses the hardware design. Practical results are presented at the end of the chapter.

Chapter 10 provides the conclusion to this thesis. Recommendations for further research are also presented.

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Chapter 2

Literature Review

This chapter reviews the different topics studied in literature, which forms the background of the remainder of the thesis.

2.1 Power Transmission & Distribution

The electric power transmission system serves as the link between energy producing power plants and the loads. Every electric power transmission system consists of three parts. These parts are the generation system, transmission system and distribution system. The generation system produces energy. The transmission system transfers the energy to the distribution system. The distribution system transfers the power to the loads [18]. Figure 2.1 shows an artist's impression of a typical power system. The illustration is provided from [1].

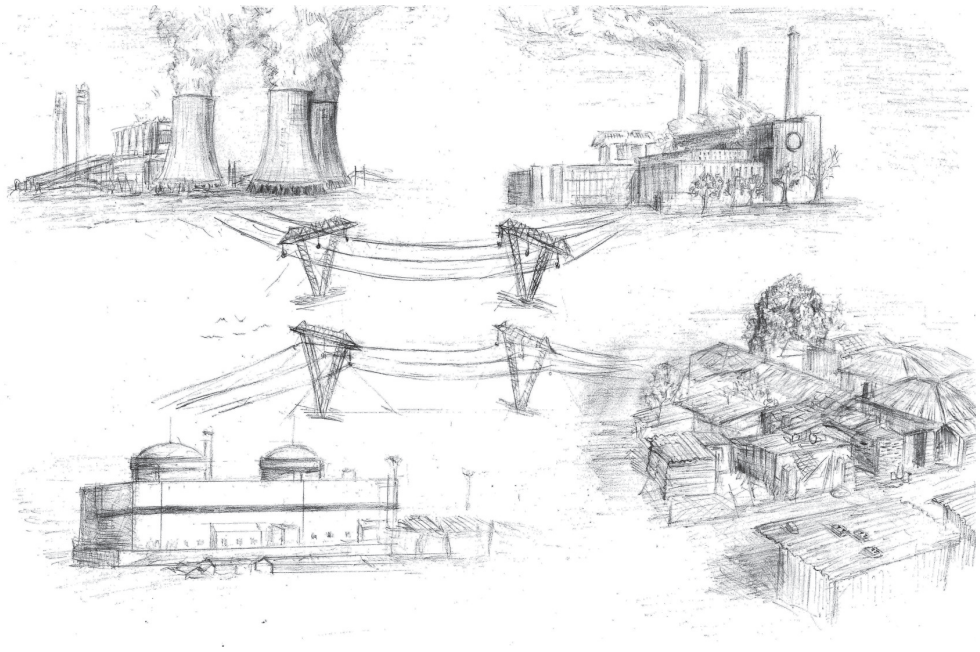

Figure 2.1 – Typical Power System from [1]

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In Figure 2.1, the generation system is shown on the left. The distribution system is shown on the right; supplying power to different kinds of loads. The transmission system is shown to connect these two systems by a line with typical 765 kV structures.

Transmission systems are mostly three-phase systems and operate at 60 Hz in the USA and at 50 Hz in Europe, Australia, parts of Asia and South Africa. The RMS voltage between the conductors are referred to as the line-to-line voltage and is used to define the system voltage [18].

Recently the need to transmit power over long distances in bulk quantities has increased and become a worldwide current topic in the energy industry. Long distance power transmission will permit the connection of remote generation centres and power grids. High Voltage Direct Current (HVDC) and half-wavelength power transmission have shown to be possible solutions. The Madeira River Hydropower Generation Project in Brazil is an excellent example of long distance bulk power transmission. This system transmits 3 150 MW through each of the two 2 400 km HVDC transmission lines [19].

A half-wavelength transmission lines have several advantages properties. The first of these is that the voltages at the sending and receiving ends are equal in magnitude and power factor. The second is that the voltage in the middle of the line is proportional to the ration of its surge impedance load and the transmitted power. The third is that the current in the middle of the line is constant regardless of the transmitted power. The fourth is that the phase shift between the sending and the receiving ends is 180°, therefore behaving similarly to a short line in regards to dynamic stability. Because of the aforementioned properties, there is no need for series or shunt compensation. Therefore the total cost will be reduced, making half-wavelength transmission a possible alternative to HVDC transmission [20].

HVDC transmission will be discussed in depth in the following section.

2.2 HVDC Transmission

2.2.1 Introduction

High Voltage Direct Current (HVDC) concerns the transmission of electrical power through the use of DC voltages instead of AC voltages. Although HVDC transmission lines are less common that their AC counterparts, HVDC transmission serves a unique purpose.

HVDC transmission is primary used for bulk long-distance power transmission, but has also been applied to underwater -power transmission, the interconnection of asynchronous power systems and stabilisation of large interconnected AC power systems.

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2.2.2 Historic Origins

The first two decades of electric power transmission witnessed several waves of pioneers. First there was Edison with the DC system. Gaulard and Ferranti followed with single-phase AC. Finally, Tesla and Dolivo-Dobrowolsky developed polyphase AC, which later developed into the three phase system we use today [21].

In 1882, Edison opened the first power station, which supplied 30 kW at 110 V DC to 59 customers [22].

Later problems were encountered as the length of transmission lines increased and the demand for power grew. The DC station could not provide a high enough voltage to mitigate the line losses [22].

In 1886, the Westinghouse Electric Company introduced the transformer to America. The company's chief engineer, William Stanley, designed the first working AC system in America. The system contained transformers and supplied power to several stores and offices [23].

Transformers facilitated the easy increasing of to voltages to a high enough level to overcome problematic line-voltage drops. This made transmission of power possible. In the light of this development, AC was favoured and became accepted as the technology of choice for transmitting power [22].

Around 1929 Dr Uno Lamm developed a device that could rectify AC at high voltage levels. In the following years much research was done on HVDC and much accomplishments were made [4]. In 1954 the first commercially successful HVDC transmission line was completed. The system operated at a voltage of 100 kV and delivered 20 MW from the Swedish mainland to the island of Gotland [4]. Since the first HVDC system was constructed, many major HVDC systems had been constructed around the world. Today the total capacity of HVDC systems exceeds 75 GW [5].

2.2.3 Comparison of HVDC and conventional transmission

HVDC transmission presents several advantages to AC transmission. These advantages are subsequently discussed.

The main advantage of a DC line is that it tends to be more economical when longer transmission lines are required. This is also the reason why HVDC first was developed. Similarly, AC lines tends to be more economical for shorter lengths. The costs of a transmission line includes the number of conductors, the need for compensation and terminal equipment. Several factors influence the cost of a transmission line albeit a DC or AC line. The total cost is divided between the set-up cost and the operational cost. The losses associated with the operation of the transmission line mainly contributes to the operational costs. The set-up cost consists of the cost of the Right of Way, supporting structures, insulators, conductors and terminal equipment. Each factor is subsequently discussed [5].

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The space required to construct a transmission line is referred to as the Right of Way. A DC transmission line requires only two conductor, where as an AC line that delivers the same power would require at least three conductors. Figure 2.2 show the comparison. As shown in Figure 2.2, a DC transmission line requires a smaller Right of Way, a simpler, and therefore a cheaper, supporting structure [6].

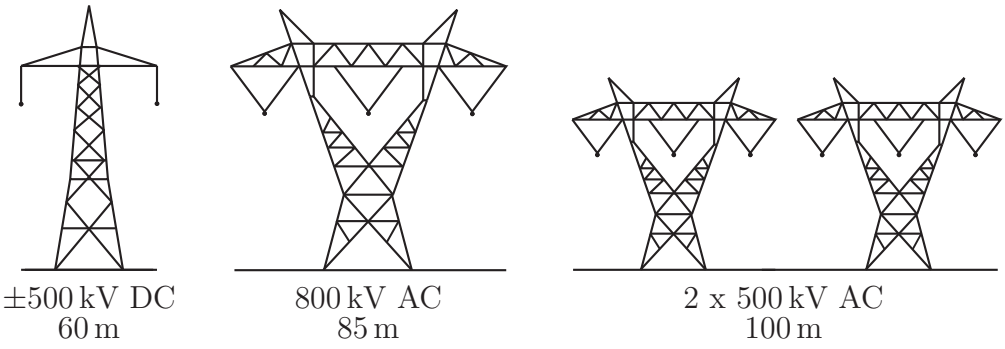

Figure 2.2 – Right of Way

The characteristics of insulators are different when DC voltages or AC voltages are applied. For simplicity, it is assumed that the characteristics of an insulator are similar when a DC or AC voltage is applied and depends on the peak voltage applied in respect to ground. Therefore it can be shown that a DC transmission line with two conductors designed for a specific insulation level can carry the same amount of power than an AC transmission line with three conductors designed for the same insulation level. This reduces the insulator costs and since DC has one less conductor, line losses are also reduced to about by a third of AC transmission line of the same power carrying capability [5].

Another benefit of a DC transmission line is that the skin effect is eliminated and the entire cross-section of the conductor is utilised. This reduced line losses marginally. Dielectric losses in power cables are also much less for a DC transmission line. Further, corona effects tend to be less significant on DC transmission line than on an AC transmission line of the same rating. This leads to a more economic choice of conductors for the construction of a DC transmission line [5].

Another factor that influences the cost of line costs are line compensation and terminal equipment. A DC transmission does not require compensation as in the case of an AC transmission line. Terminal equipment required for a DC transmission line include converters and filters, and therefore are more expensive than the required terminal equipment for a AC transmission line [5].

There is a length of line where a DC and an AC line would cost the same to set-up. An AC transmission tends to be more economical for shorter lengths of line and a DC transmission line tends to be more economical for longer lengths. This is referred to as the break even distance.

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Depending on the per unit price of the conductors, the break even distance vary between 400 km to 700 km for overhead line and 25 km to 50 km for a cable system [6]. Figure 2.3 shows the break even distance for an AC transmission overhead line and a DC transmission overhead line.

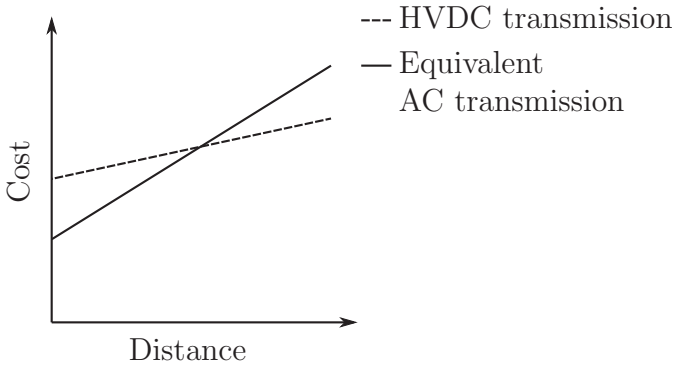

Figure 2.3 – Break Even Distance

A DC transmission line has several advantageous technical characteristics that are not found in a AC transmission line. These characteristics are mainly attributed to the fast controllability of power that is achieved by the converter control. These advantages are firstly the full control of the power transmitted, secondly the enhanced transient and small signal stability in the associated AC networks and lastly the fast control allows the limiting of fault currents, making it feasible to avoid DC breakers.

DC power transmission overcomes some of the problems associated with AC power transmission. These problems are stability limits, voltage control, line compensation, AC power network interconnection and ground impedance issues. The issues are each subsequently discussed.

The amount of transmitted power in an AC transmission line is dependent on the angle difference in voltage phasors on each side of the transmission line. As the angle difference increases, so the transmitted power increases. The maximum angle difference is limited by steady state and transient stability conditions. The maximum power that can be transmitted on an AC transmission line decrease as the length the transmission line increases. The amount of power transmitted on a DC transmission line is only limited by the current carrying capability of the conductor. This capability is also referred to as the thermal limit of the transmission line. The length of a DC transmission does not affect the steady state and transient stability. Figure 2.4 shows the power transfer capabilities of both a DC and an AC transmission line.

Voltage control in an AC transmission line is complicated because of the charging of the line and inductive voltage drops. DC transmission converter stations require reactive power, but the transmission line itself does not. AC cable transmission lines require steady-state charging currents, but DC cable transmission systems do not.

As mentioned above, an AC transmission line requires compensation to increase power transfer capability and to improve stability limitations. Series capacitors and shunt inductors are used

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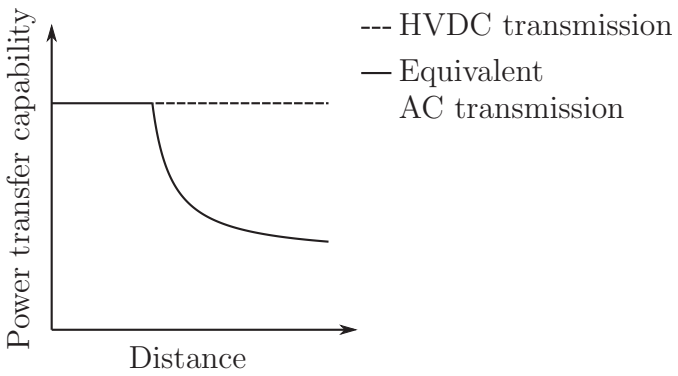

Figure 2.4 – Power Transfer Capabilities

for line compensation. Another option is to use a Static VAR Compensator (SVC). Line compensation is especially important for underwater cables. A DC transmission line does not require compensation, therefore making it suitable for underwater cable power transmission systems.

The synchronous interconnection of AC power systems can be problematic. Coordination between the generation control of both systems is required to achieve an interconnection. Problems associated with synchronous interconnection, even with coordination, includes frequent tripping because of the presence of large power oscillations, fault levels increasing and disturbances being transmitted from one system to the other. A DC interconnection eliminates the need for coordination and all of the problems mentioned above. A DC interconnection could even connect power systems that operate at different nominal frequencies.

In AC transmission systems, ground currents, also known as zero sequence currents, can not be allow in steady-state. Because of the high magnitude of ground impedance, efficient power transfer will not be possible. Another consequence of ground currents is telephonic interference. For DC currents, the ground impedance is negligible. Therefore a DC transmission line can operate with only one conductor and a ground return. The only problem with a DC transmission line using a ground return is the corrosion of metallic objects buried in the current path.

According to [6], the reliability of DC transmission systems are good and comparable to AC transmission systems. Further it is quoted that the availability of DC transmission lines are far above 90%.

The application of DC transmission systems are limited because of several factors. These are the breaking of DC currents, transformers cannot be used to change voltage levels, the high cost of converter equipment, additional filters required because of the converters generating harmonics on the AC and DC side, the reactive power requirement and the complexity of the control.

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2.2.4 Workings of a HVDC transmission system

A typical HVDC transmission system can be represented by two voltage sources and a transmission line. This representation is shown in Figure 2.5. The transmission line is represented by the resistor. The arrow indicated the desired direction of current flow.

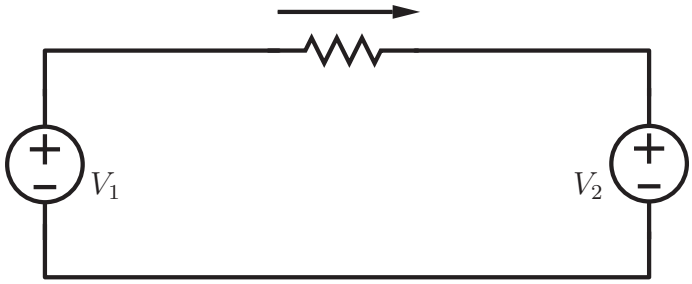

Figure 2.5 – Typical HVDC Transmission Thyristor Converter

Power flows from the left hand voltage source (V_1) to the voltage source on the right hand side (V_2). To achieve this, the voltage source V_1 must be larger than the voltage source V_2. The amount of power transmitted is determined by the difference in voltages on both sides. In practice, each voltage source is referred to as a terminal. Each terminal consists of the following components: converter bridge consisting of several switches, transformers, smoothing reactor and filters [24]. The converter that converter AC to DC is represented by the voltage source V_1 and referred to as the rectifier terminal. Similarly, the converter that converters the DC voltage to AC voltage are referred to as the inverter terminal. A typical HVDC transmission terminal is shown in Figure 2.6. The workings of the converters are discussed in detail in the subsequent Section 2.2.6.

High DC voltages are generated by rectifying high AC voltages. Transformers are used to step up these voltages, provide isolation between rectifiers and provide phase shifts in voltages should phase shifts be necessary [24].

The converter causes harmonics on the AC- and DC sides of the converter. DC Filters are used to attenuate these harmonics on the transmission line. On the AC side, filters and power factor correction equipment are used to attenuate harmonics and provide the reactive power required by the converters. A smoothing reactor is connected to smooth the line current and for protection purposes [24]

Typically, the rectifier terminal is under constant current control and the inverter terminal is under constant voltage control. This arrangement facilitates constant power transfer.

This is a simple system representation used to illustrate the basic principles of HVDC transmission systems. Several other more complex system are used in practice and is discussed in subsequent sections.

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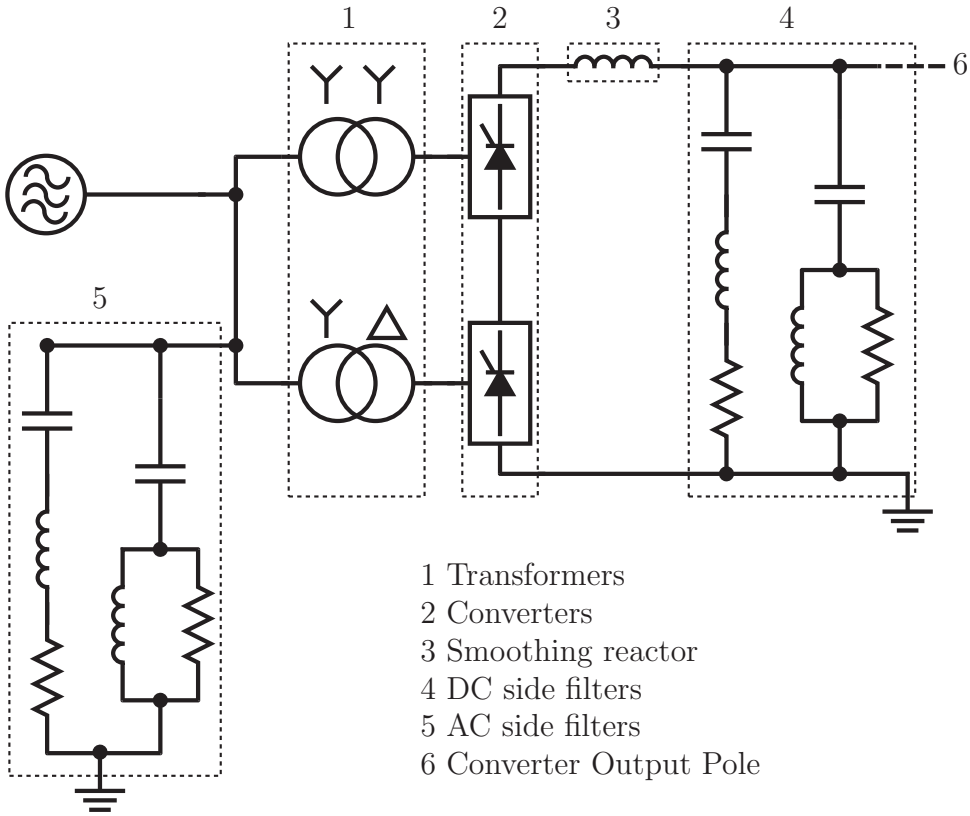

Figure 2.6 – Typical HVDC Transmission Thyristor Converter

2.2.5 Configurations or Types

HVDC transmission was originally used as a point-to-point technology, but shortly after the operation of systems with more than two terminals was investigated. Point-to-point transmission systems can be connected and operated in three different modes. These are known as the monopolar, bipolar and homopolar configuration. Figures 2.7, 2.8 and 2.9 shows the different configurations. Some of the configurations make use of Single Wire Earth Return technology. An earth return is indicated by a dotted line. A solid line represents a line conductor [5].

The monopolar configuration uses a single conductor and an earth return. A metallic return is used to avoid corrosion or harmonic interference. In HVDC cable systems, the cable return is used. The conductor is mostly operated at negative polarity since DC corona effect are substantially less than for positive polarity [6].

The bipolar configuration uses two conductors, one at positive polarity and one at negative polarity. For Extra High Voltage applications the conductors could be bundled conductor [5]. Each terminal has two sets of converters that has the same current and voltage rating. The connection between the two sets of converters is grounded. Under normal operating conditions each conductors carries equal current and therefore there is zero ground current flowing. Monopolar operation can be used under faulty converter conditions [6].

Homopolar configuration uses two or more conductors operated at the same polarity and uses an earth or metallic return. The conductors are usually operated as the negative pole [5]. An

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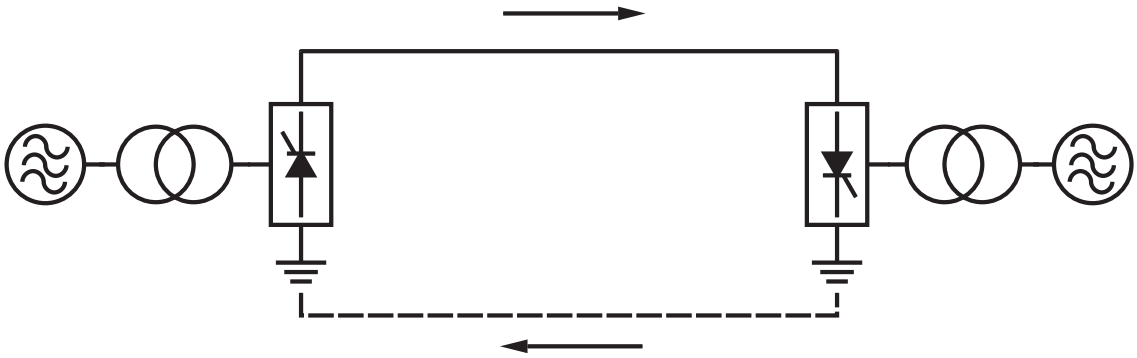

Figure 2.7 – Monopolar Configuration

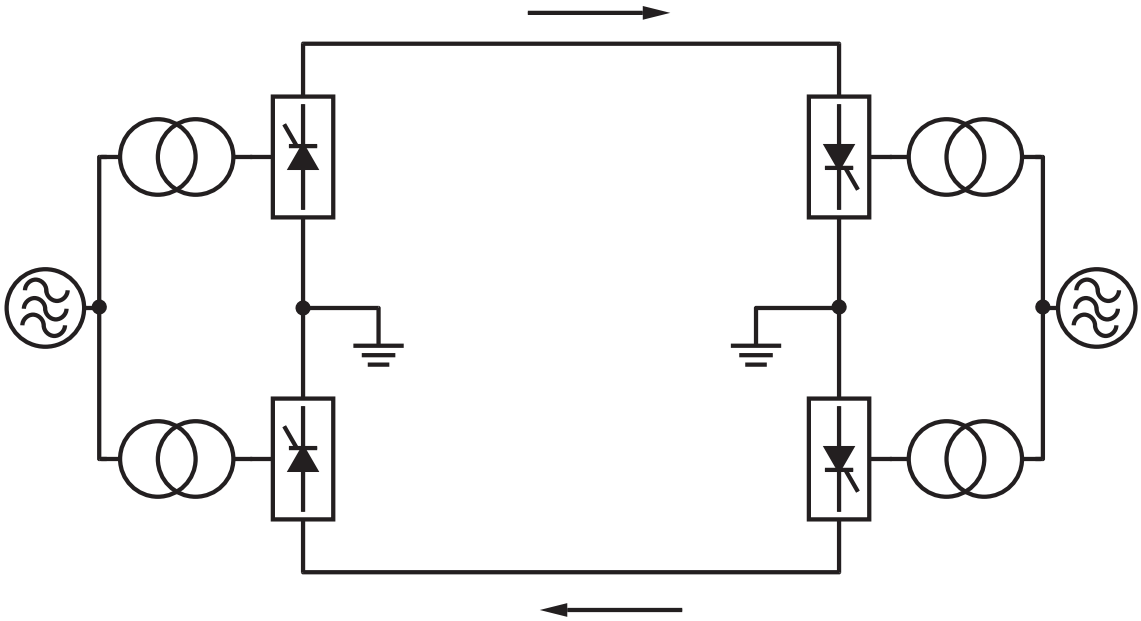

Figure 2.8 – Bipolar Configuration

interesting advantage of the homopolar configuration is that of reduced insulation costs [6].

Bipolar configurations are mostly used because of the disadvantages associated with ground return.

An HVDC transmission consisting of more than two terminal are referred to as Multi-Terminal HVDC, also known as MTDC. Papers discussing realistic strategies for achieving multi-terminal operation have been published since 1963 [7]. Currently there are only two multi-terminal schemes that is in operation. These schemes are in Corsica and Canada [5].

The first HVDC multi-terminal to enter commercial operation is the Sardinia-Corsica-Italy HVDC project, also known as SACOI. The project started operations in 1987 [8]. Originally the project was rated at 200 MW, but in 1992 the power rating was upgraded to 300 MW [25].

The Québec - New England HVDC project was commissioned from 1990 to 1992. The project consists of three poles and the total power rating of the project is 2 000 MW. The project is due for an upgrade in 2016 [26].

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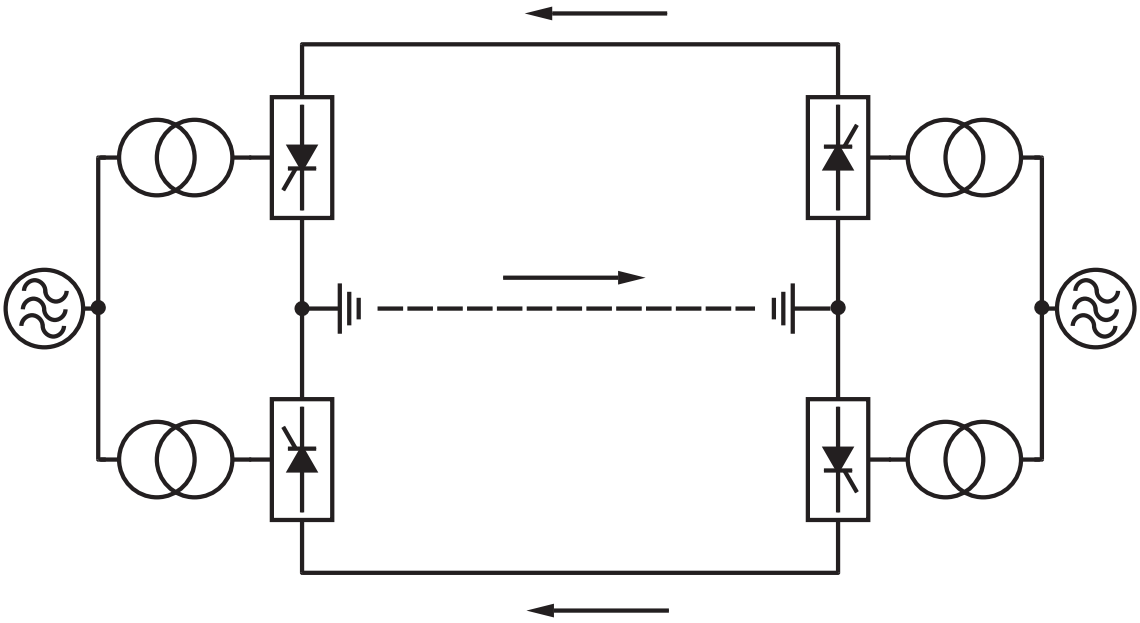

Figure 2.9 – Homopolar Configuration

The terminals of a MTDC system can be configured in several different ways. Additional terminals can be connected in series or parallel. A parallel MTDC system can also be of the radial or mesh type. A MTDC system that has additional terminals connected in series and parallel is referred to a hybrid system. Figure 2.10 shows how the different configurations relate to each other.

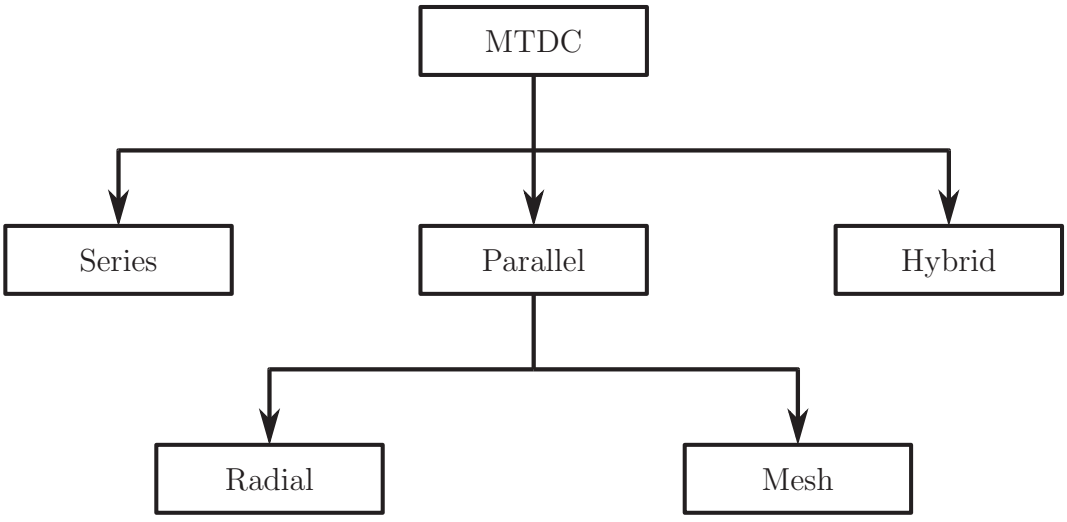

Figure 2.10 – MTDC Configurations

A three terminal series MTDC configuration is shown in Figure 2.11. A two terminal HVDC system is extended by connecting a third terminal in series to the original two terminals. The figure shows a monopolar configuration, but a series MTDC system is also possible with other configurations. In a series MTDC system, the current is set by one converter terminal and

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is common to all terminals. The other terminals operate under voltage control to deliver the required power from the HVDC transmission line.

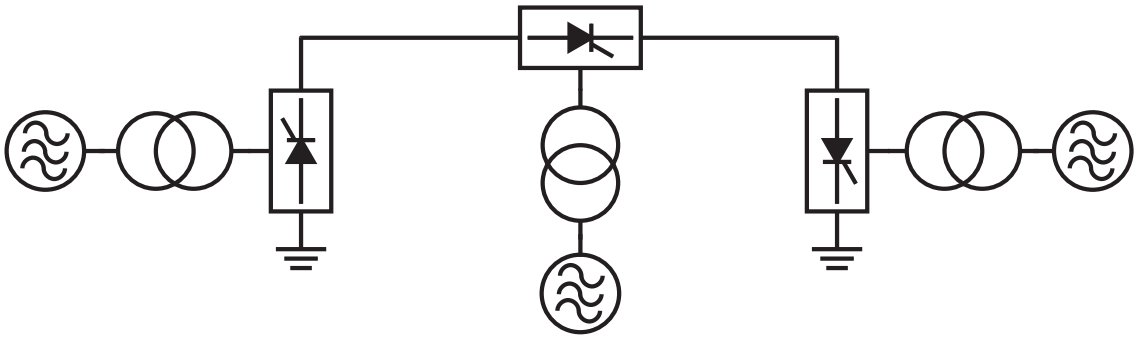

Figure 2.11 – MTDC Series Configuration

In Figure 2.12, a three terminal radial parallel MTDC system is shown. A radial parallel configuration in achieved by connecting a third terminal in parallel to a two terminal HVDC system. One of the terminal operates under voltage control. The voltage is common to all the terminals in the MTDC system.

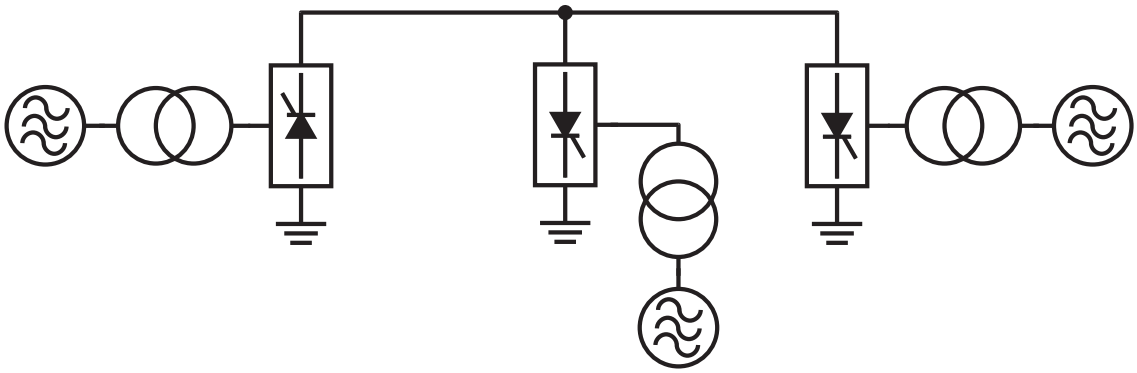

Figure 2.12 – MTDC Parallel - Radial Configuration

In a radial MTDC system, disconnection of one segment would lead to loss of power to one or more terminals. Should a segment be lost in a mesh MTDC system, power will not be lost to the terminals in the system provided the remaining links have the required power rating. Therefore, a mesh parallel MTDC system could be considered more reliable than a radial parallel MTDC system. A 4-terminal mesh parallel MTDC is shown in Figure 2.13.

As previously mentioned, there are only two MTDC schemes operational in the world, as discussed in [8] and [26]. Both of these schemes are in parallel configuration. Another application of parallel configuration might be the interconnection of off shore wind farms, as described in [27]. In [28], the management and viability of such systems are investigated.

Series MTDC and parallel MTDC system each has its own advantages and disadvantages. A brief comparison between these MTDC systems follows subsequently. High speed reversal of power flow without the need for mechanical switching is possible with a series MTDC system.

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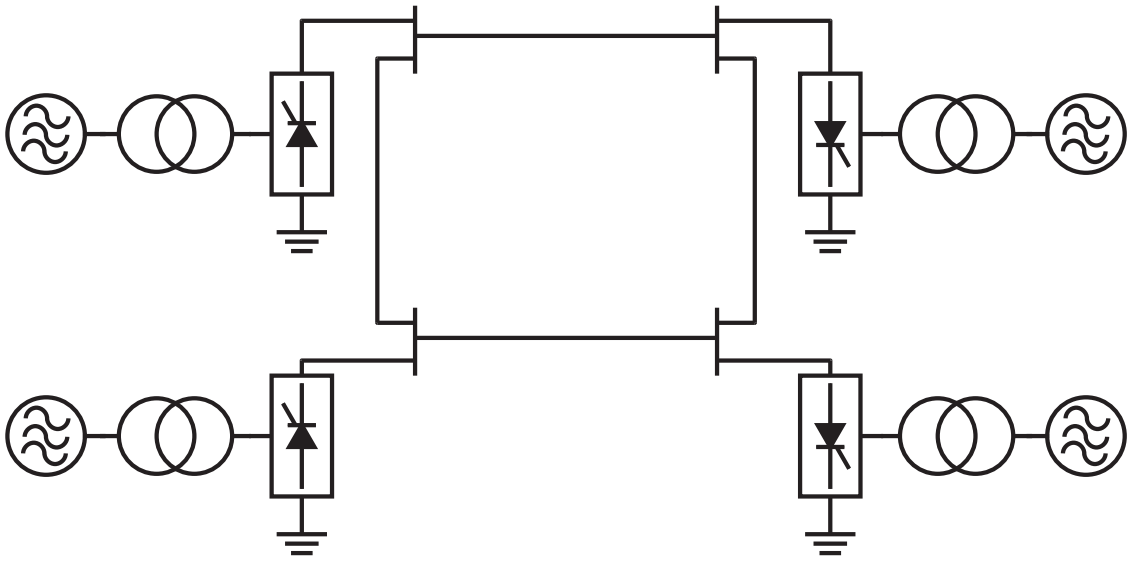

Figure 2.13 – MTDC Parallel - Mesh Configuration

The voltage rating of the switching in a series terminal is dependent on the power rating of the terminal, although the switches will need to be isolated from ground potential. The switches used in a parallel terminal must be rated for the full system voltage. Insulation coordination is more complex because the voltage of the system varies along the line. Control and protection of a series MTDC system is a natural extension of a two terminal HVDC system. A parallel MTDC system is a more complicated matter of increased communication requirements.

From the advantages and disadvantages of each MTDC configuration, it may be concluded that a series terminal is appropriate for a power rating of 20 % of the system power rating.

As mentioned above, a hybrid MTDC system is a MTDC system consisting of a combination of series and parallel connected terminals. Such a MTDC system have not been implemented in practice but has been successfully simulated as shown in [10].

Multi-Infeed HVDC systems are several HVDC terminal that share a common AC bus and that have a small impedance between the different HVDC converters. Figure 2.14 shows a typical Multi-Infeed HVDC system. Multi-Infeed HVDC systems share some of the problems associated with Multi-Terminal HVDC operation [5]. Mutual interaction of the different HVDC converters because of DC- or AC-side disturbances poses serious concerns. Interactions could occur through voltage distortion, phase imbalance and amplitude- or phase changes. The consequences of these interactions lead to degraded performance of each of the HVDC converters. The main problems that could be encountered are control interactions causing small signal instability, voltage instability and collapse, increased commutation failures because of AC faults occurring on a neighbouring HVDC converter and transient AC voltage dips because of simultaneous recovery of HVDC converters after AC faults [29].

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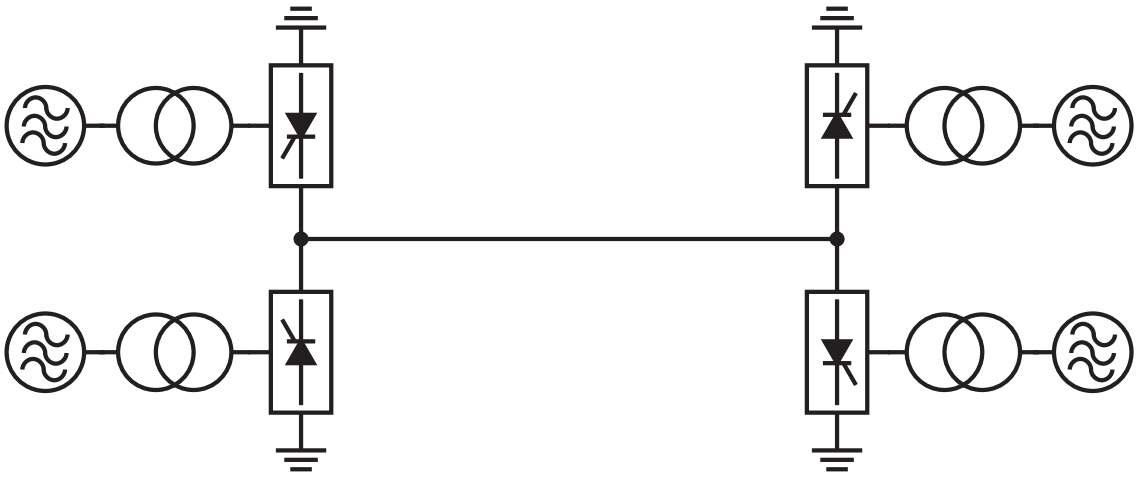

Figure 2.14 – Multi-Infeed

2.2.6 Converter types and Switching devices

Through out the history of HVDC transmission, several different converter types have been used to rectify and invert at high voltage. Just as different types of converters have been used, several different switching devices are associated with each converter type. HVDC converters can be divided into two main groups. These groups are Line Commutated Converters (LCC) and Voltage Source Converters (VSC) [5].

Line Commutated Converters utilises the line voltage connected on the AC side of the converter to aid in commutation of the switches. Such switches include Mercury Arc Valves and Thyristors. From 1950 to 1990, the Line Commutated Converter configuration was the most common [6]. The first device that was able to rectify at high voltage was the mercury arc valve. This device was invented by Udo Lamm, who pioneered HVDC [4]. Mercury Arc Valves was mainly used in Line Commutated Converters from the early 1950s to mid-1970s. Figure 2.15 shows a photo of a Mercury Arc Valve taken by the author. Thereafter the thyristor replaced the mercury arc valve as the main switching device used in Line Commutated Converters [6]. Refurbishment projects have been implemented to replace mercury arc valves with thyristor valves. Thyristors also does not suffer flashbacks, a major fault that does occur in mercury arc valves. An example of such a project is the Nelson-River HVDC project [30].

Voltage Source Converters utilises switches that can commutate by themselves without the aid of the AC connected line voltage. These converters have been available since 1990. Such devices include IGBTs and GTOs. Voltage Source Converters acts as a voltage source on the DC side of the converter [6].

Line Commutated Converters and Voltage Source Converters uses the same basic configuration of switches. This configuration is known as the Graetz bridge. Figure 2.16 shows the configuration of a three-phase converter commonly used on HVDC converters. The switches are numbered in the order that they are switched assuming a positive phase rotation [5]. The number of switches are referred to as the pulse number. Figure 2.16 therefore shows a six-pulse

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Figure 2.15 – The Mercury Arc Valve

converter.

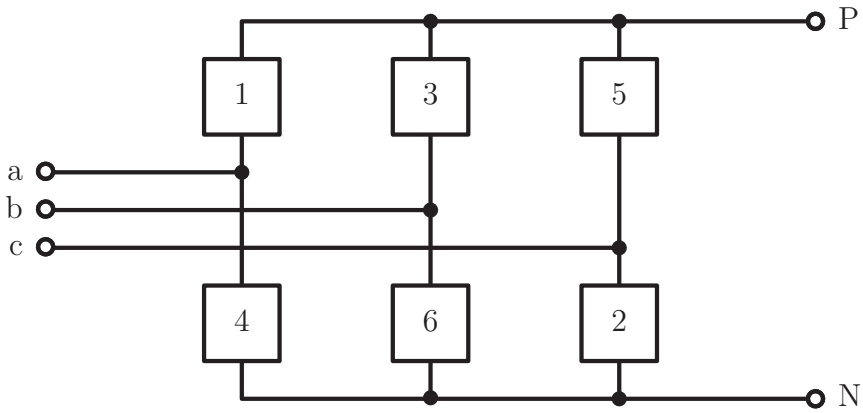

Figure 2.16 – The Graetz Bridge

A converter acting as a current source or voltage source on the DC side of the converter, depends on the type of switch used in the Graetz bridge, the switching scheme and the type of converter control used [5].

Only thyristor based converters will be used in this thesis. These voltages are connected to terminals a, b and c, as seen in Figure 2.16. The DC voltage appears across terminals P and N. Thyristor converters varies the average output voltage by delaying the firing of the thyristors. In the case of three phase converters, this delay is defined as the time from when of one supply phase to neutral voltage becomes larger its preceding phase to the time that the corresponding

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thyristor is fired. This time is called the firing angle of the converter. The symbol α is used for the firing angle. Should the switches indicted in Figure 2.16 be replaced with thyristors, the type converter will be referred to as a six-pulse converter. This type of converter is commonly used to rectifier three phase voltage. The average DC voltage of a six-pulse thyristor converter is given by Equation 2.2.1. The derivation is given in [31].

$$V_{rectifier} = \frac{3\sqrt{2}}{\pi} V_{LL} \cos(\alpha) \tag{2.2.1}$$

Should the firing angle be $0° < \alpha < 90°$, the converter is operating as a rectifier. The converter is operating as an inverter should the firing angle be $90° < \alpha < 180°$. The angle of advance of an inverter is defined as $\beta = \pi - \alpha$. The average DC voltage of a thyristor inverter is given by Equation 2.2.2. The derivation is given in [24].

$$V_{inverter} = \frac{3\sqrt{2}}{\pi} V_{LL} \cos(\beta) \tag{2.2.2}$$

Equations 2.2.1 and 2.2.4 assumes current transfers instantaneously between thyristors fired in successive order.

Because of line inductances and self inductances of the transformers present at the AC side of a thyristor converter, current takes a finite time to commutate between thyristors fired in successive order. This time is referred to as the commutation angle (u). The length of the commutation angle is affected by the size of the inductances and the magnitude of the current flowing through these inductances. Equation 2.2.3 shows the equation for the average DC voltage of a six-pulse thyristor rectifier taking the commutation angle into account. The commutation angle is affected by the supply inductance (L_s) present on the AC-side, load current (I_d) of the rectifier and operating frequency (ω) of the rectifier.

$$V_{rectifier} = \frac{3\sqrt{2}}{\pi} V_{LL} \cos(\alpha) - \frac{3\omega L_s I_d}{\pi} \tag{2.2.3}$$

In order to switch a thyristor off, the current through the device must fall under the holding current for a certain period before the thyristor can block a forward voltage. This period is referred to as the turn-off time. The turn-off time consists of reverse recovery time and gate recovery time. Should the thyristor experience an increase in current before the turn-off time has elapsed, the thyristor may spontaneously turn on again.

For inverter operation, the angle of advance is kept to as low as possible to minimise reactive power consumption. To simplify calculations, the inverter equation is often expressed in terms of the extinction angle, defined as $\gamma = \pi - \alpha - u$. Equation 2.2.4 shows that for inverter operation, the extinction angle can be substituted for the firing angle into the rectifier equation.

$$V_{inverter} = \frac{3\sqrt{2}}{\pi} V_{LL} \cos(\gamma) \tag{2.2.4}$$

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All of the above equations are derived for six pulse converters. Higher number pulse converters can also be configured. Twelve pulse converters are commonly used on HVDC terminal converters. Higher pulse number converters present the advantage of lower output voltage- and current harmonics. The higher the pulse number, the smaller the phase difference between the supply AC voltages must be. Transformers connected in star-to-star and star-to-delta are used to create the necessary phase difference between the supply voltages required by a twelve pulse converter.

2.2.7 HVDC Control

The purpose of an HVDC transmission system is to deliver constant power according to a power order. Constant power transfer can be achieved by controlling either the voltage or current. From the viewpoint of minimisation of line losses, the voltage of the HVDC line should be kept constant and the current must be adjusted to meet the required power. This strategy also improves voltage regulation and allows the optimal use of insulation. The voltage drop along a DC line is less than with an equivalent AC line because a DC line does not have a reactive voltage drop [5].

Figure 2.17 shows the equivalent circuit of a HVDC transmission line. The two voltage sources V_{DCrev} and V_{DCinv} are the voltages appearing across the rectifier converter and the inverter converter respectively. The value of the voltage is defined by Equations 2.2.1 and 2.2.4 [5].

Equations 2.2.1 shows that the DC voltage across the rectifier (V_{DCrev}) is influenced by the firing angle (α) of the converter and the AC voltage supplied (V_{ACrec}) to the converter. In a similar manner, Equation 2.2.4 shows that the DC voltage (V_{DCinv}) across the inverter is influenced by the extinction angle (γ) of the converter and the AC voltage (V_{ACrec}) to the converter. In turn, the AC voltages are influenced by the tap settings of the transformers. Therefore the control variables available are α, γ, V_{ACrec} and V_{ACinv} [5].

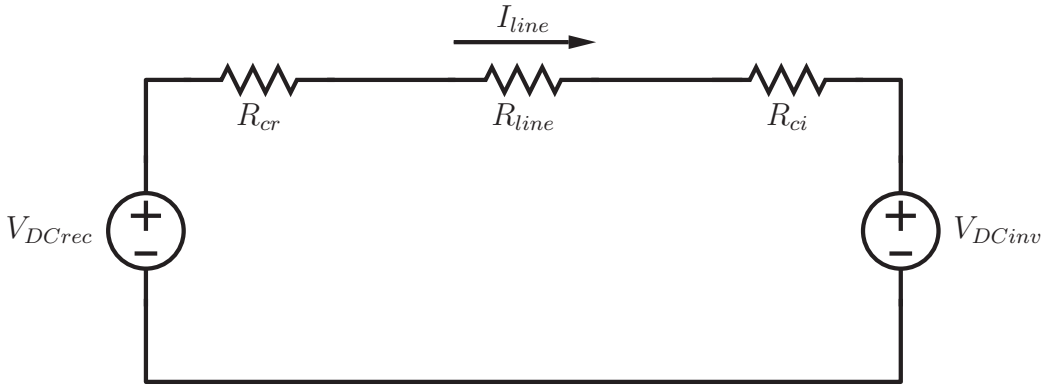

Figure 2.17 – Control Equivalent

By Ohm's Law, the line current is given by Equation 2.2.5 [5].

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$$I_{line} = \frac{V_{rectifier} - V_{inverter}}{R_{cr} + R_{line} + R_{ci}} \tag{2.2.5}$$

The resistance R_{line} is the resistance of the line. The resistances R_{cr} and R_{ci} are called equivalent commutation resistances and are defined as

$$R_{cr} = \frac{3}{\pi} X_{cr}$$
$$R_{ci} = \frac{3}{\pi} X_{ci}$$

with the leakage inductances if the transformers defined as X_{cr} and X_{ci} [5].

To achieve constant power transfer under normal conditions, the rectifier is operated under constant current control using Equation 2.2.5 and the inverter is operated under constant voltage control using Equation 2.2.4. Subsequently, the inverter determines the line voltage of the HVDC line and the rectifier will determine the line current of the HVDC line. Different control schemes are implemented at each converter to achieve constant power transfer. An in depth discussion of these different schemes are beyond the scope of this thesis [5].

A hierarchy of controls are used in a HVDC transmission system. Such a hierarchy is shown in Figure 2.18.

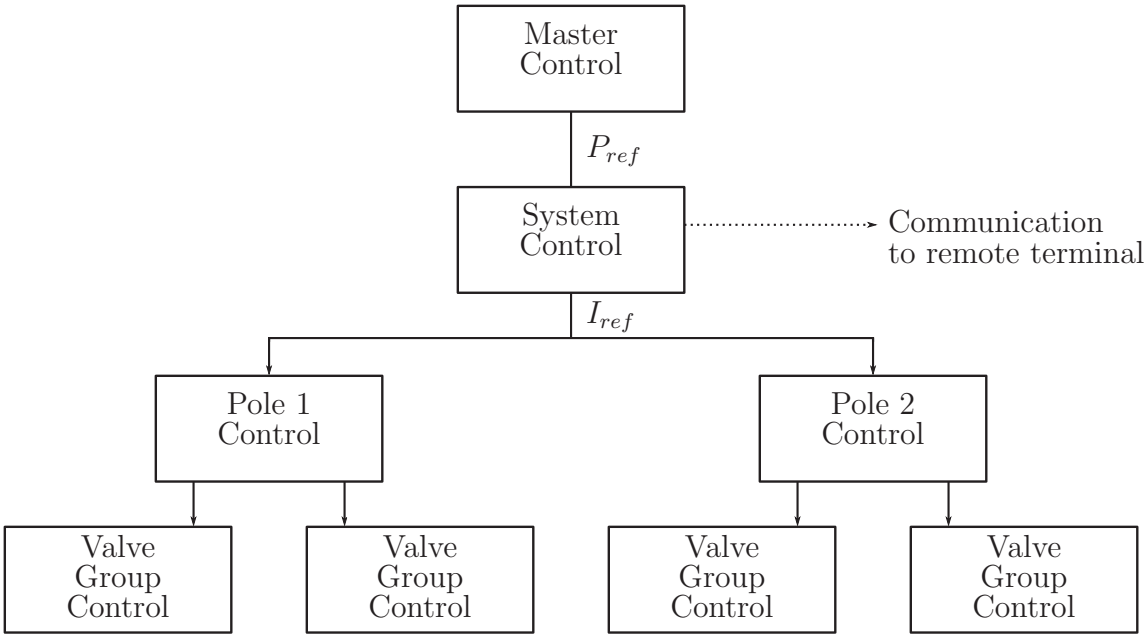

Figure 2.18 – Control Hierarchy

The System Control issues a power order (P_{ref}) according to the conditions of the power system that the HVDC transmission system is connected to. The Master Control issues a current order (I_{ref}) to the Pole Controllers. The Pole Controllers in turn issues firing angle orders to the individual Valve Group Controller [5].

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2.2.8 Harmonics

Harmonics are generated during the conversion process. These harmonics are injected on both the AC and the DC side of the converter. There are several problems that is caused by the presence of harmonics. These include telephone interference, extra power losses, resonances causing overvoltages, instability of converter controls and interference with ripple control systems [5].

For HVDC converters, harmonics can be divided into characteristic harmonics and non-characteristic harmonics.

Characteristic harmonics are generated by the conversion process and is always present even if the AC supply voltages are balanced and the pulses are equi-distant. The DC current is assumed to be constant because of the large inductance of the smoothing reactor. In such a case the order of the AC current harmonics (h_{AC}) are given by Equation 2.2.6, with p_n the pulse number of the converter and n equal or larger than one [5].

$$h_{AC} = np_n \pm 1 \tag{2.2.6}$$

The order of the harmonics present on the DC side is given by Equation 2.2.7, with with p_n the pulse number of the converter and n equal or larger than one. Given that the smoothing reactor only has a finite inductance, harmonics of the same order given in Equation 2.2.7 will be present [5].

$$h_{DC} = np_n \tag{2.2.7}$$

Any harmonics that occurs at any other order than that of the characteristic harmonics are called non-characteristic harmonics. These harmonics are caused by imbalance of the two converters that make a 12-pulse converter, firing angle errors, unbalance and distortion in the AC supply voltages and unequal transformer leakage impedances [5].

Tuned filters are typically used for the filtering of specific harmonics present on the DC and AC side of the converter. Passive and active filtering solution have been suggested, as described in [32].

The design of these filters are beyond the scope of this thesis and is described in [33].

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2.2.9 Notable HVDC Projects

The total installed capacity of HVDC projects exceeds 75 000 MW [5]. Some of the more notable projects are described below.

- *Itaipu*
  The Itaipu project operates at ±600 kV and consists of four poles. It delivers 6300 MW to São Paulo. It is one of the largest HVDC overhead transmission projects [34].

- *Québec - New England*
  The Québec - New England projects is one of the only two multiterminal HVDC projects in the world. It was the first to be upgraded. The project is rated at 2000 MW. The two poles operate at ±450 kV [26] [35].

- *SAPEI*
  The SAPEI HVDC projects is the largest HVDC link in the Mediterranean Sea. HVDC is used because of the length of sea cable. The link operates at ±500 kV. The project is rated at 1000 MW and has two poles [8] [36].

- *NorNed*
  The NorNed link connects Norway to the Netherlands. It is the longest undersea HVDC project. Two cables is used to reduce cable losses. A single cable is 580 km long. The project has only one pole and is rated at 700 MW [37].

- *Gezhouba-Shanghai*
  The Gezhouba-Shanghai HVDC operates at ±800 kV. The line delivers 6400 MW [38].

2.2.10 Modern Trends

Some of the modern developments in HVDC is described below.

DC Breakers
Modified AC switchgear is typically used to break small DC current. These pieces equipment is employed as disconnection switches. DC breakers or Metallic Return Transfer Breakers are used to break rated load currents [5]. In 2012, ABB released a report of a HVDC breaker that uses mechanical and semiconductor technology to achieve ultra-fast operation and negligible conduction losses [39].

Conversion of existing AC lines
Some utilities are investigating the option to convert AC lines to DC lines to achieve higher power transfer for the same Right of Way. A double circuit AC line can be converted to a bipolar HVDC line to achieve a power transfer increase of about 3.5 times [5].

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Operation with weak AC systems

Conventional thyristor converters are not compatible with weak AC systems because the thyristors require a strong AC system to facilitate commutation. With the event of self commutating devices, for example IGBTs, being used in HVDC converters allows the converter to be connected to weak AC networks [5].

Deep Hole Earth Electrode

The earth electrode of HVDC systems plays an important role. Deep Hole Earth Electrodes are used should a convenient grounding point not be available. Instead of using a large area of land of high resistivity earth, a Deep Hole Earth Electrode is used. These electrodes are installed approximately 500 m to 1000 m below the ground. This will ensure that the electrode will be in low resistivity soil. The electrode element is between 100 m to 200 m long. Deep Hole Earth Electrodes allows for easy location of earthing site, closer location of the electrode to the converter station and enhanced possibilities to operate the HVDC link in monopolar mode [6].

HVDC Transmission using IGBT based converters

ABB delivers a product known as HVDC Light that utilises IGBT based converters to perform the rectification and inversion at the terminals of a HVDC scheme [40]. Siemens delivers a similar product known as HVDC PLUS (Power Link Universal System) [41].

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2.3 The Cahora-Bassa HVDC Transmission System

The Cahora-Bassa HVDC transmission system went into full commercial operation in July 1979. This system supplied South Africa with hydroelectricity. The civil war in Mozambique lead to sporadic interruptions of operations on the line. These interruptions were caused by acts of sabotage. These acts started in 1982 and continued until operation on the line stopped in 1985. Recommissioning of the line started in 1997 once the political situation in Mozambique has stabilised [32].

The Cahora-Bassa system delivers 1 919 MW from Mozambique to South Africa. The line current is 1 800 A and the line operates at ±533 kV. The rectifier station is called Songo and the inverter station is called Apollo. Figure 2.19 shows the map where the stations and the line are situated. The line starts in the North of Mozambique, runs along the Zimbabwe-Mozambique border and ends in the North of South Africa. The picture is taken from [2].

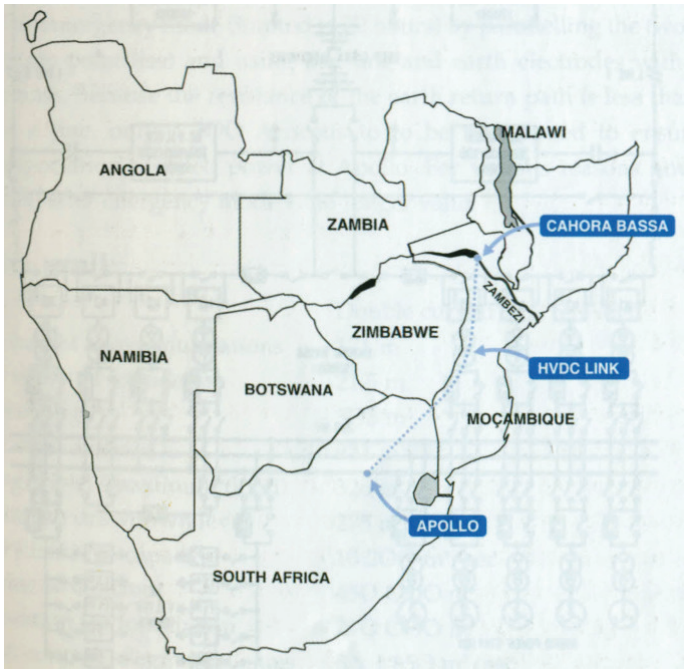

Figure 2.19 – Map of the Cahora-Bassa Line from [2]

Figure 2.20 shows a diagram of the Cahora-Bassa line. At the Cahora-Bassa Generation Station, five 480 MVA machines generate power. A 220 kV AC line transmits the power to the Songo rectifier station 6 km away. The Songo Rectifier Station transmits the power through two lines situated a 1 km apart. The voltage of these line are ±533 kV DC. The Apollo Inverter Station receives the power 1414 km away. There the power is introduced to the Eskom Power System at 275 kV AC [2]. The Cahora-Bassa HVDC transmission system is primarily operated in bipolar mode. In the event that one of the lines are not available, the remaining available line will be operated in monopolar mode. This mode only allows half of the rated power to be delivered. The different modes of operation is described in Section 2.2.5. The figure is taken from [32].

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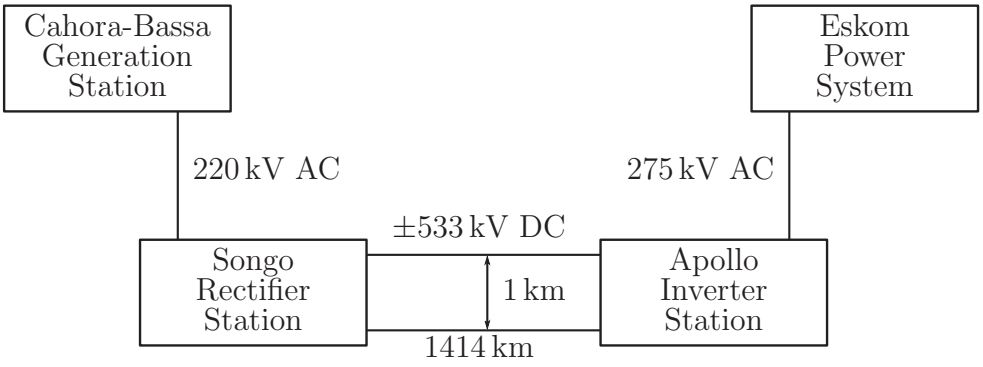

Figure 2.20 – Diagram of the Cahora-Bassa System

Figure 2.21 shows the dimensions of the pole structure used on the Cahora-Bassa HVDC transmission line, as shown in [32]. The earth wire is constructed of Oden conductor, consisting of twelve 3,52 mm aliminium strands and seven 3,52 mm steel strands. Zambezi conductor, consisting of forty-two 4,14 mm aluminium strands and seven 2,32 mm steel strands, is used for the main conductor. The main conductor uses 4 conductors, each 45 cm apart.

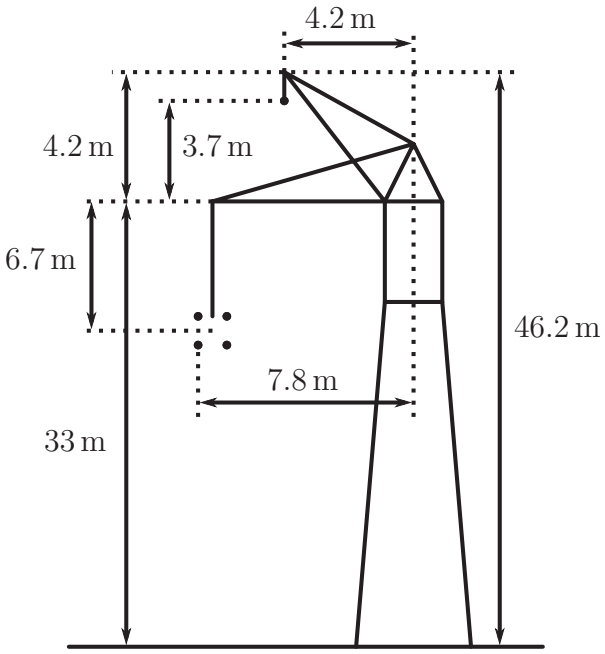

Figure 2.21 – Cahora-Bassa Pole Structure from [2]

Figures 2.22, 2.23, 2.24 and 2.25 shows photographs taken of the Cahora-Bassa HVDC transmission line in Mozambique. The photographs were provided by [3]

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Figure 2.22 – A photo of the Cahora Bassa line next to the road. Provided by [3]

Figure 2.23 – A photo of the Cahora Bassa line. Provided by [3]

Figure 2.24 – A photo of a single pole structure. Provided by [3]

Figure 2.25 – Several visible pole structures of the Cahora Bassa Line. Provided by [3]

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In Figure 2.26, a more detailed diagram of the specific setup of the Cahora-Bassa HVDC Transmission System is shown. The specific hardware configuration can be observed to contain four transformers per pole, two configured in star to star and two in star to delta. Each transformer feeds a thyristor converter bridge. Figure 2.26 also shows the different filters connected to the Cahora-Bassa HVDC transmission System. Each converter has a DC and AC filter bank. The placement of switchgear can also be seen [2].

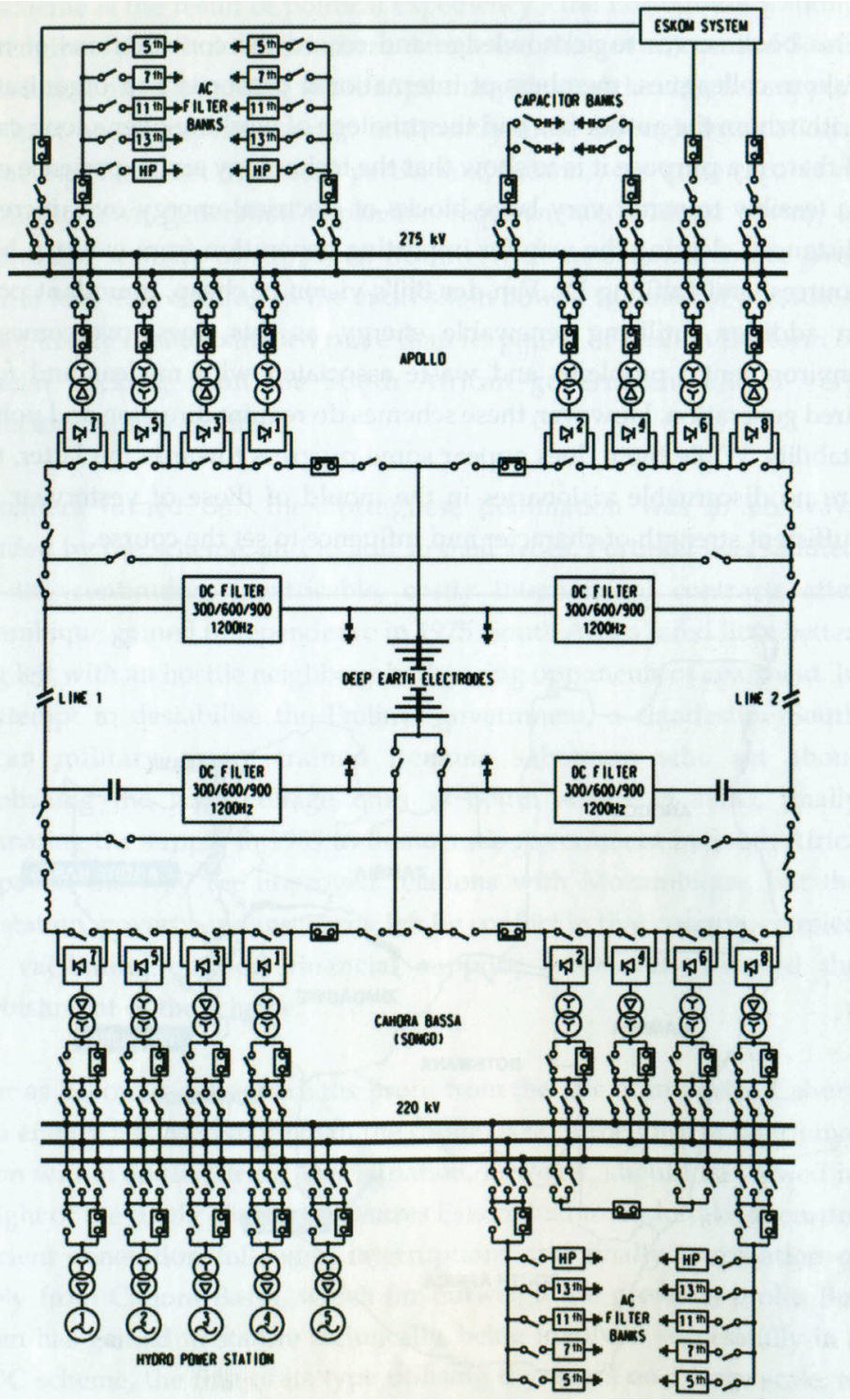

Figure 2.26 – Cahora-Bassa Converter Diagram from [2]

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Chapter 3

HVDC Terminals Model Hardware Design

3.1 Introduction

Construction of a HVDC Terminals model in hardware is proposed to investigate and better understand the behaviour of a typical HVDC transmission system. The particular behaviour that is of paramount importance is the harmonics present on the line and the control of both the converters.

The design approach used concerns several stages of design. The first step is to make a list of specifications. A system level design is then carried out to ensure the that the system will reach the different specifications. Thereafter, each individual component of the system will be designed and individually tested. The individual components will then be interconnected and the entire system will be tested.

The specifications of the HVDC will be specified first. A system level design will then be performed. The design will be confirmed in simulation. Subsequently, the design and construction of the different pieces of hardware used to create a practical setup will be discussed. The chapter concludes with practical measurements to ensure that the HVDC Terminals model functions within the specifications.

3.2 HVDC Terminals Model Specifications

The following section defines the hardware specifications of the HVDC Terminals model at the system level. The specification were made based on how HVDC transmission systems look in practice, the need to keep construction costs as low as possible and the available laboratory equipment.

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The Cahora-Bassa HVDC transmission system was chosen as a case study to base the HVDC Terminals model on. The Cahora-Bassa system was studied in Section 2.3. Figure 2.26 shows the setup of the Cahora-Bassa system. The Cahora-Bassa HVDC Terminals is a bipolar configured system. For the purpose of studying the HVDC Terminals model, only a monopole will be required. The same information can be acquired from a monopolar model than from a bipolar model. The decision is further motivated to reduce construction costs of the model. Since the impedance for a ground return is negligible for DC currents, the earth return of the model will be modelled by a short circuit.

It is decided that each three single-phase transformers will be connected together to form a single three-phase transformer. Such a set of three single-phase transformers, forming a single three-phase transformer, is referred to as a transformer bank. In Figure 2.26, the Cahora-Bassa is shown to use four transformer banks at each converter; two connected in star and the other two connected in delta. Four transformer banks are used to provide the required isolation and the required redundancy necessary for maintenance. The model will only use two transformer banks at each converter. Two transformer banks will be used to provide isolation between the thyristor bridges and to provide the required phase shift for 12-pulse operation of the thyristor bridges.

Thyristors will be used as the switches for the terminals. The rectifier terminal will use a thyristor rectifier. Similarly, the inverter terminal will be use a thyristor inverter. Collectively, the thyristor rectifier and thyristor inverter are called thyristor converters.

The firing angle of the thyristor rectifier is chosen as 30° and firing angle of the thyristor inverter is chosen as 150°. The chosen fire angle allows the thyristor converter a wide enough control range before the firing angle becomes to large. Larger firing angles lead to more reactive power being draw from the source. The power factor of the power drawn from the source should be as close to unity power factor as possible. Therefore the firing angles should be kept as low as possible.

The filters and smoothing reactor will be constructed using the same values found in the Cahora-Bassa system.

The purpose of the HVDC Terminals Model is to study the behaviour of a HVDC transmission system and not the study of the model of a DC transmission line. For simplicity the transmission line was chosen to be represented by a resistance.

Given the voltages and currents that can be generated by the available equipment, a set of system ratings is chosen. Table 3.1 shows the summarised specifications that were decided upon.

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Rectifier DC voltage	V_{DCrec}	600 V
Inverter DC voltage	V_{DCinv}	450 V
Line current	I_{line}	3 A
Line Resistance	R_{line}	50 Ω
Rectifier Firing Angle	α_r	30°
Inverter Firing Angle	α_i	150°

Table 3.1 – Model System Specifications

Figure 3.1 shows the schematic of the HVDC transmission system and the definitions of voltages and currents are shown.

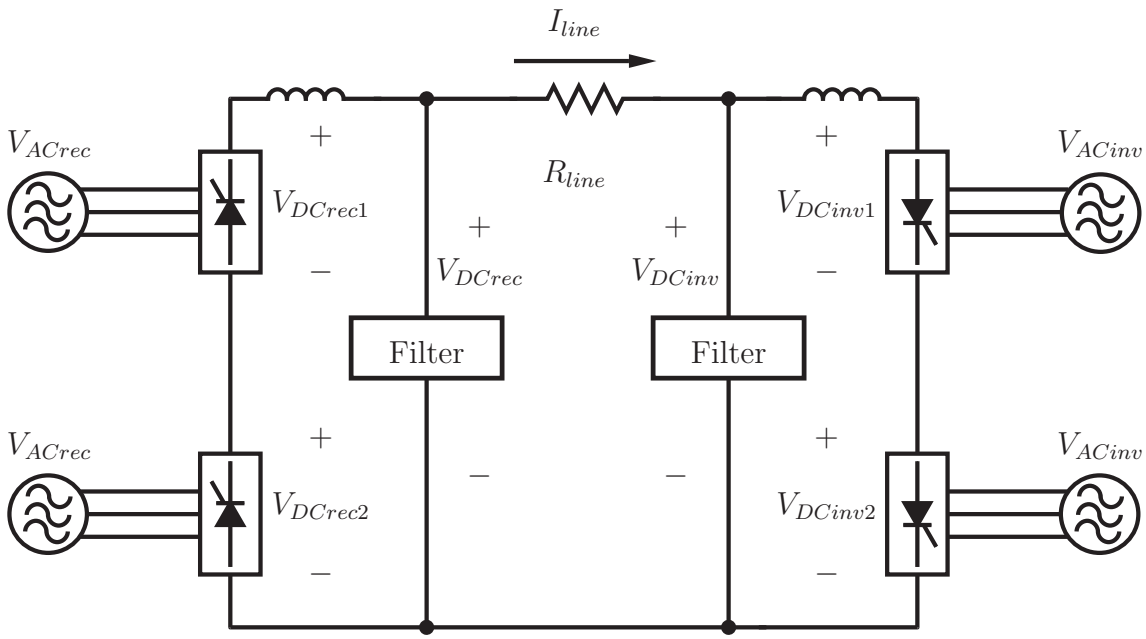

Figure 3.1 – Model Schematic

3.3 Model System Design

3.3.1 Overview

In the previous section, several specifications concerning the HVDC Terminals model was made. These specifications need to be implemented in a practical model. According to the design approach discussed in Section 3.1, after the specifications have been made, a system level design must be made to realise the specifications in a practical model. Thereafter the design must be confirmed with a system level simulation.

3.3.2 System Level Design

The system level design values are supply AC voltages. It is assumed that the voltages are divided equally among the two six-pulse converters. The delta-star connected transformer

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bank will feed the top six-pulse converter. The star-star connected transformer bank will be connected to the lower six-pulse converter. Further it is assumed that the phase-to-phase voltages (V_{LL}) on the secondary side of each of the transformer bank will be the of equal voltage. Therefore, every voltage supplying a thyristor converter will be of equal magnitude and only a single AC supply voltage will have to calculated.

The design will then be confirmed in simulation. From the simulation required component ratings can be decided upon.

The required AC voltages needs to be calculated using the firing angle. The equation that relates the AC line-to-line supply voltage (V_{LL}) and firing angle to the average DC output voltage ($V_{rectifier}$) is given by Equation 3.3.1. This equation is discussed in Section 2.2.6

$$V_{rectifier} = \frac{3\sqrt{2}}{\pi} V_{LL} \cos(\alpha) \tag{3.3.1}$$

As stated before, each six pulse thyristor six-pulse bridge will supply half of the required DC voltage at each converter. Therefore $V_{DCrec1} = V_{DCrec2} = 0.5V_{DCrec}$ and $V_{DCinv1} = V_{DCinv2} = 0.5V_{DCinv}$.

To obtain the rectifier equation, substitute $0.5V_{DCrec}$ for $V_{rectifier}$ and V_{ACrec} for V_{LL} into Equation 3.3.1. To simplify the control of the inverter, the inverter will be controlled using the fire angle instead the angle of advance. It is assumed that the commutation angle will be negligible. Therefore the equation for the inverter can be obtained by following the same process and substituting $0.5V_{DCinv}$ for $V_{rectifier}$ and V_{ACinv} for V_{LL} into Equation 3.3.1. Equations 3.3.2 and 3.3.3 shows the resulting equations, with α_r defined as the firing angle for the rectifier and α_i defined as the firing angle of the inverter.

$$V_{DCrec} = 2\frac{3\sqrt{2}}{\pi} V_{ACrec} \cos(\alpha_r) \text{ for } 0^\circ < \alpha_r < 90^\circ \tag{3.3.2}$$

$$V_{DCinv} = -2\frac{3\sqrt{2}}{\pi} V_{ACinv} \cos(\alpha_i) \text{ for } 90^\circ < \alpha_i < 180^\circ \tag{3.3.3}$$

Using Equations 3.3.2, the AC supply voltage for the rectifier can be calculated. Equation 3.3.4 shows the result.

$$\begin{aligned} V_{ACrec} &= \frac{\pi}{6\sqrt{2}\cos(\alpha_r)} V_{DCrec1} \\ &= 257\,\text{V} \end{aligned} \tag{3.3.4}$$

This voltage will be supplied using a variac that is available in the laboratory.

By following the same calculation and using Equation 3.3.3, the AC supply voltage for the inverter can be calculated. Equation 3.3.5 shows the result.

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$$V_{ACinv} = -\frac{\pi}{6\sqrt{2}\cos(\alpha_i)} V_{DCinv1} \tag{3.3.5}$$
$$= 192\,\mathrm{V}$$

3.3.3 Transformer Tests

Before a system level simulation can be performed, the inductances present on the AC side of the converter need to be determined. These inductances are important to determine if the commutation angle of the converter is negligible, as assumed above.

It is assumed that the inductances present on the AC side (L_s) are dominated by the transformers' leakage inductances (X_{eq}). The transformer leakage inductances will be determined using an equivalent transformer model. The equivalent transformer model proposed in [22] will be used. The parameters of the transformer model cannot be measured directly and will be determined by performing open- and short circuit tests and then calculating the model parameters based on the results of the tests. The only parameter that is of interest is the leakage inductance and the winding losses. Therefore only short circuit tests will be performed.

Figure 3.2 shows the equivalent transformer model. The left hand side is the primary side and the right hand side is the secondary side. The equivalent series impedance is the sum of the primary series impedance and the secondary series impedance that has been referred to the primary side. The equivalent series impedance represents the winding copper losses (R_{eq}) and the flux leakage (X_{eq}). The shunt branches models the magnetising current (B_m) and core losses (G_c).

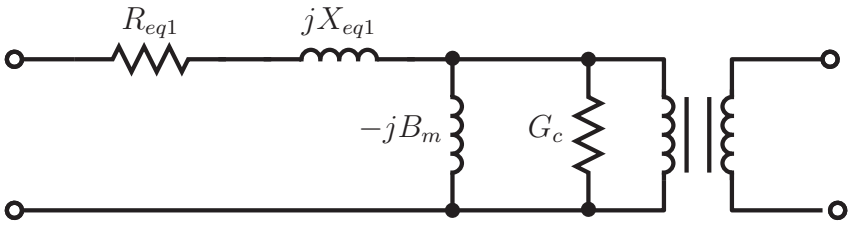

Figure 3.2 – Equivalent Transformer Model

Only the equivalent series inductance (X_{eq}) and series resistance (R_{eq}) of the different transformers will be calculated to determine if the commutation angle and the series resistances are negligible. Therefore, only the short circuit test will be performed. The test setup is shown in Figure 3.3. The secondary winding is shorted out and the rated current is applied to the primary winding. The voltage across the primary winding and the real power delivered to transformer is measured for use in the calculation of the equivalent series impedance. The shunt branches are neglected for the short circuit test. The short circuit test will be performed at 50 Hz; the same frequency that will be used to supply the transformers.

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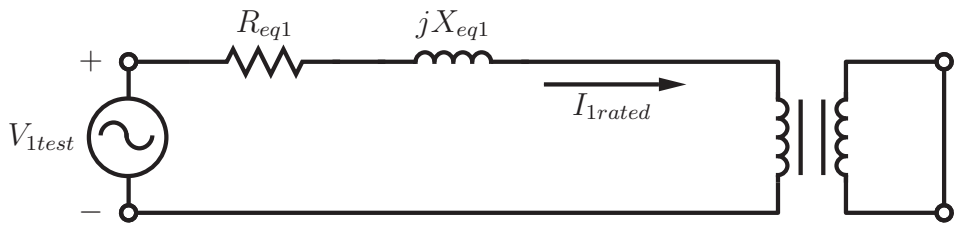

Figure 3.3 – Short Circuit Test

The following procedure is followed to calculate the rated current, series resistance and series inductance.

Equation 3.3.6 shows the rated current (I_{1rated}) is calculated by dividing the total power rating of the transformer (S_{rated}) by the rated voltage of the primary winding (V_{1rated}).

$$I_{1rated} = \frac{S_{rated}}{V_{1rated}} \tag{3.3.6}$$

The series resistance (R_{eq}) is calculated by dividing the real power delivered to the transformer through the primary winding (P_1) by the rated current (I_{1rated}), as shown by Equation 3.3.7.

$$R_{eq} = \frac{P_1}{{I_{1rated}}^2} \tag{3.3.7}$$

Equation 3.3.8 shows the magnitude of the impedance (Z_{eq}) is calculated by the rated current (I_{1rated}) and the measured voltage across the primary winding (V_{1test}).

$$|Z_{eq}| = \frac{V_{1test}}{I_{1rated}} \tag{3.3.8}$$

The equivalent series reactance (X_{eq}) is the calculated using Equation 3.3.9

$$X_{eq} = \sqrt{{Z_{eq}}^2 - {R_{eq}}^2} \tag{3.3.9}$$

Equation 3.3.10 shows the total equivalent impedance (Z_{eq}) as the sum of its real and imaginary components.

$$Z_{eq} = R_{eq} + jX_{eq} \tag{3.3.10}$$

The imaginary part of the impedance can be converted to an inductance with Equation 3.3.11 with $f = 50\,\text{Hz}$.

$$L_{eq} = \frac{X_{eq}}{2\pi f} \tag{3.3.11}$$

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According to [22], the leakage inductances are assumed constant for rated and near rated operating conditions. The model does not take saturation, inrush current, non-sinusoidal exciting current or surge phenomena into account.

Table 3.2 shows the measured real power (P_1), current (I_{1rated}) and voltage (V_{1rated}) for each transformer on the left of the double horizontal line. The calculated equivalent series resistance (R_{eq}) and inductance (L_{eq}) is shown on the right of the double horizontal line.

No	V_{1rated}	V_{2rated}	S_{rated}	I_{1rated}	V_{1test}	P_1	R_{eq}	X_{eq}	L_{eq}
1	253 V	244 V	1200 VA	4.756 A	9.71 V	37 W	1.636 Ω	j1.222 Ω	3.889 mH
2	253 V	244 V	1200 VA	4.763 A	9.60 V	38 W	1.675 Ω	j1.121 Ω	3.568 mH
3	253 V	244 V	1200 VA	4.779 A	9.63 V	38 W	1.664 Ω	j1.137 Ω	3.618 mH
4	440 V	244 V	1200 VA	2.719 A	15.13 V	36 W	4.869 Ω	j2.693 Ω	8.572 mH
5	440 V	244 V	1200 VA	2.746 A	15.42 V	37 W	4.907 Ω	j2.731 Ω	8.692 mH
6	440 V	244 V	1200 VA	2.717 A	15.39 V	36 W	4.877 Ω	j2.881 Ω	9.172 mH
7	253 V	244 V	1200 VA	4.753 A	9.55 V	37 W	1.638 Ω	j1.164 Ω	3.705 mH
8	253 V	244 V	1200 VA	4.759 A	9.87 V	38 W	1.680 Ω	j1.218 Ω	3.878 mH
9	253 V	244 V	1200 VA	4.762 A	9.65 V	38 W	1.676 Ω	j1.139 Ω	3.627 mH
10	440 V	244 V	1200 VA	2.736 A	15.35 V	36 W	4.809 Ω	j2.889 Ω	9.197 mH
11	440 V	244 V	1200 VA	2.722 A	15.23 V	36 W	4.859 Ω	j2.775 Ω	8.832 mH
12	440 V	244 V	1200 VA	2.737 A	15.44 V	36 W	4.806 Ω	j2.954 Ω	9.404 mH

Table 3.2 – Short Circuit Test Results

The practical inter-connection of these transformers is discussed in Section 3.4.8.

The commutation angle is calculated by the Equation 3.3.12.

$$\cos(\alpha + u) = \cos(\alpha) - \frac{\sqrt{2}\omega L_s I_d}{V_{LL}} \tag{3.3.12}$$

The variance in the values of the leakage inductance are subscribed to tolerances in the manufacturing process. The leakage inductance of the single-phase transformers used for the delta-star connected transformer bank has higher leakage inductance because they have more windings than the transformers used for the star-star connected transformer bank. Because the supply voltage and load current is the same for each transformer bank, the commutation angle will be the same for each transformer bank. Each transformer bank will be treated as a single case. Therefore there are four cases to be calculated. The largest commutation angle is calculated for each case.

The load current (I_d) for all cases are 3 A. For the two cases regarding the thyristor rectifier the supply voltage (V_{LL}) is 257 V. Similarly, the supply voltage is 192 V for the two cases regarding the inverter. The delta-star connected transformers each has a leakage inductance of $L_s = 9.404$ mH and the star-star connected transformers each has a leakage inductance of $L_s = 3.889$ mH.

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Using the values specified above, the commutation angle for the two six-pulse thyristor rectifiers and the two six-pulse thyristor inverters will be calculated. The rectifier commutation angles are the first two values listed; the inverter commutation angles are listed afterwards. The delta-star connected converters are listed first and third. The calculated values are 5.19°, 2.24°, 8.64° and 3.26°. All of these values are small enough to be negligible.

3.3.4 System Level Simulation

Simplorer 15 is chosen as software of choice for the system level simulation of the HVDC Terminals model. The system specifications mentioned in Section 3.2 is simulated. Figure 3.4 shows a screenshot of the workspace in Simplorer 15.

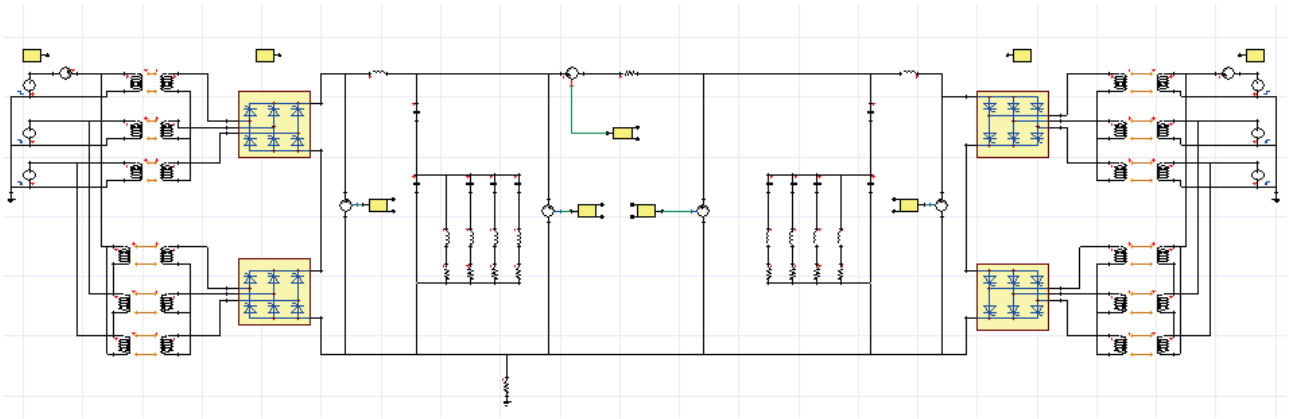

Figure 3.4 – Simplorer Setup Screenshot

Table 3.3 shows the simulation parameters. The component values are the same as described in Sections 3.4.6 and 3.4.7.

Total time	1500 ms
Minimum time step	1 μs
Maximum time step	10 μs

Table 3.3 – Simulation Parameters

To assure that the thyristor are fired at the correct firing angles, the supply voltages and the relevant thyristor voltage is shown in Figure 3.5.

The solid and dashed grey traces indicates the supply voltages. The solid black trace is the voltage across the thyristor (V_{th}). Once the thyristor has been fired, the voltage across the thyristor becomes zero. The firing angle of the rectifier is indicated. The duration of the firing angle is 1.67 ms, which is equivalent to 30° at 50 Hz. Therefore it is concluded that the thyristors are firing correctly.

The results of importance is the specifications mentioned in Section 3.2. These are the DC voltage present at the rectifier V_{DCrec} (shown in Figures 3.6 and 3.7), the DC voltage present at the inverter V_{DCinv} (shown in Figures 3.8 and 3.9) and the current flowing through the transmission line I_{line} (shown in Figures 3.10 and 3.11). The grey trace shows the instantaneous

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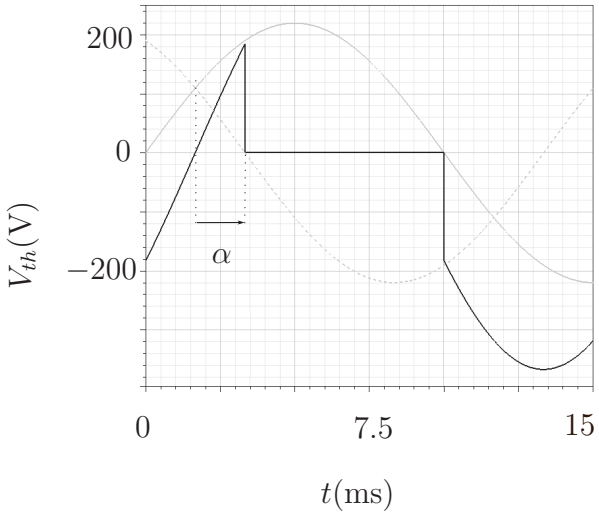

Figure 3.5 – Firing angle

voltage and the black trace shows the mean value with an averaging period of 20 ms calculated through simulation. All results presented are in steady-state.

The voltage V_{DCrec} has the expected mean value of 602 V and has a 20 V peak-to-peak ripple voltage. Similarly, the voltage V_{DCrec} has the mean value of 452 V and has a ripple voltage present of 20 V peak-to-peak. The current I_{line} has a mean value of 2.99 A and a ripple current of 30 mA. The small difference in the simulated and design values is ascribed to errors occurring because of rounding off of decimals.

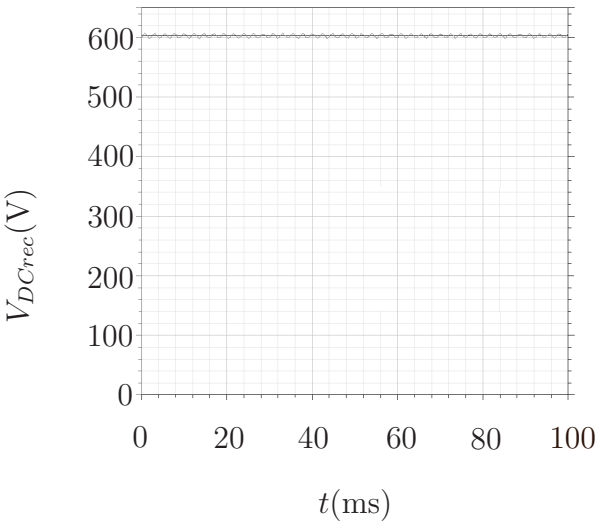

Figure 3.6 – Simulated V_{DCrec} in Steady-state

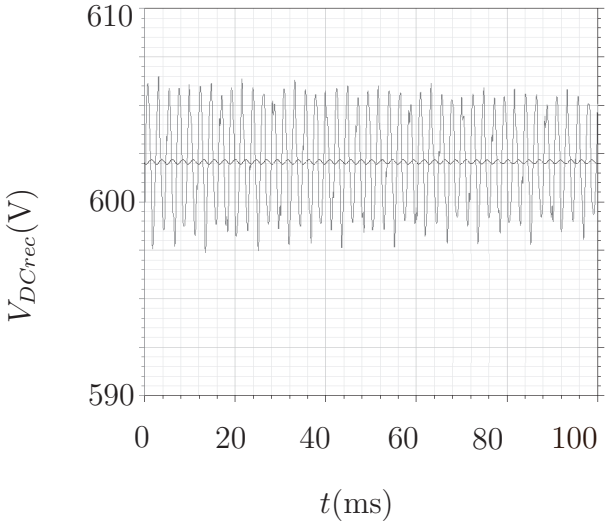

Figure 3.7 – Simulated V_{DCrec} in Steady-state - Enlarged

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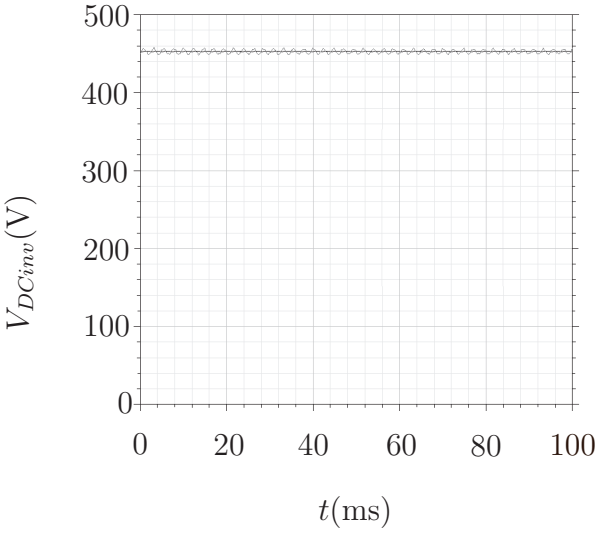

Figure 3.8 – Simulated V_{DCinv} in Steady-state

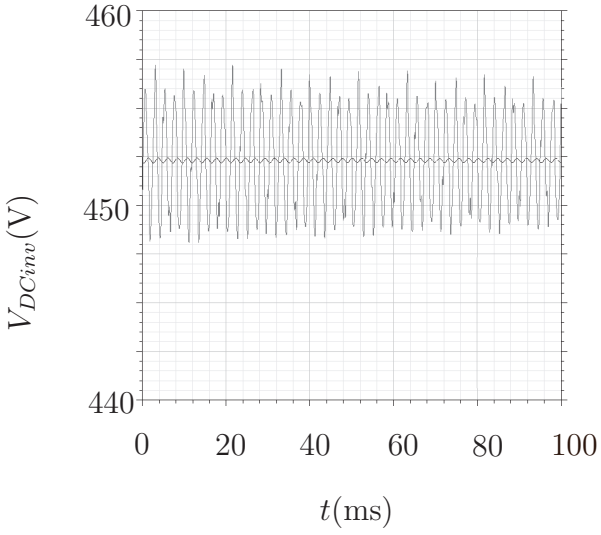

Figure 3.9 – Simulated V_{DCinv} in Steady-state - Enlarged

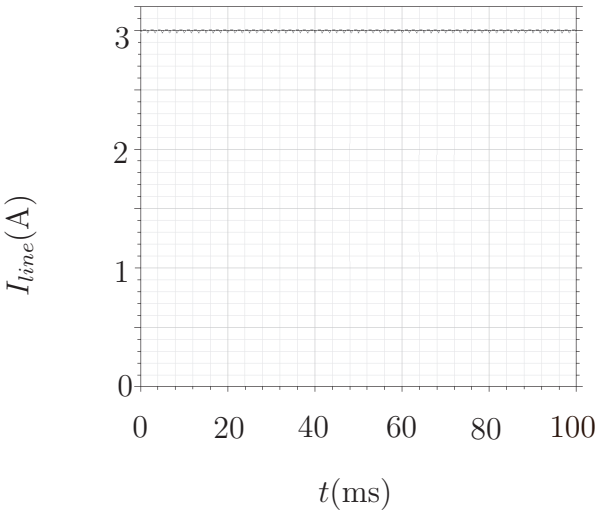

Figure 3.10 – Simulated I_{line} in Steady-state

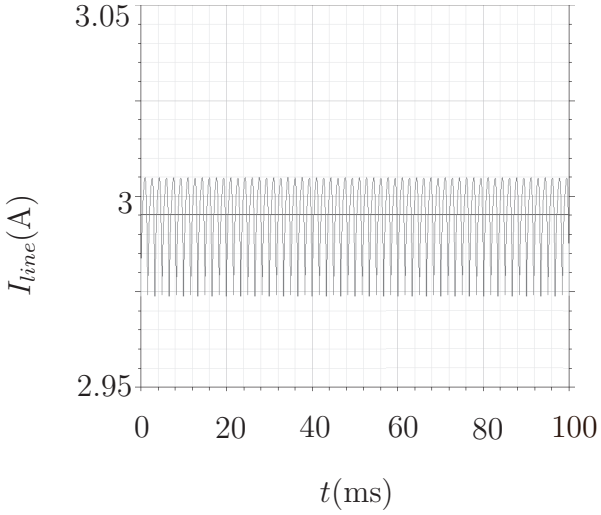

Figure 3.11 – Simulated I_{line} in Steady-state - Enlarged

3.3.5 Conclusion

A set of system specifications is chosen. These specification is successfully simulated. The simulation results gave more insight into the working of the system and provided information needed for further development.

The commutation angle is small enough to be ignored in further controller design considerations. The commutation angle is small because of low supply inductances and low load current.

It is concluded that a simulation of the HVDC Terminals have been successfully completed. Practical construction can proceed.

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3.4 Hardware Design

3.4.1 Overview

The subsequent sections discuss the design and construction of the individual pieces of hardware that form the smaller parts of the system.

In Figure 3.12 shows the hardware setup that is required to practically implement the HVDC Terminals model that was designed and simulated in the section above. The main power path is indicated by the thick solid line and is used to process the power being transferred. These pieces of hardware in the main energy path are the transformers, thyristor bridges and line model.

The transformer banks are used to create two sets of three-phase voltages that are 30° out of phase and isolated from each other.

The thyristor bridges are used to convert the supply AC voltages to the line DC voltage and inverter the line DC voltage back to an AC voltage.

The smoothing reactor is used to filter the line current and keep it relatively constant. The line filter are used to filter the most dominant harmonics on the line generated by the thyristor bridges.

Hardware used to facilitate the operation of the hardware found in the main power path, is referred to as supporting hardware. These pieces of hardware are the thyristor drivers, snubbers, the measurement boards, interface board and the control board.

The thyristor drivers are used to fire the thyristor as logic signals are received. The snubbers are used to protect the thyristors against over-voltages and prevent them to switch on spontaneously. The measurement boards are used to convert voltages and currents to signals that can be processed by the control board. The interface board serves as the link between the control board and the thyristor driver circuits. The control board generates the gate pulses in accordance with current and voltage measurements and a control law that will be designed and implemented in the following chapter.

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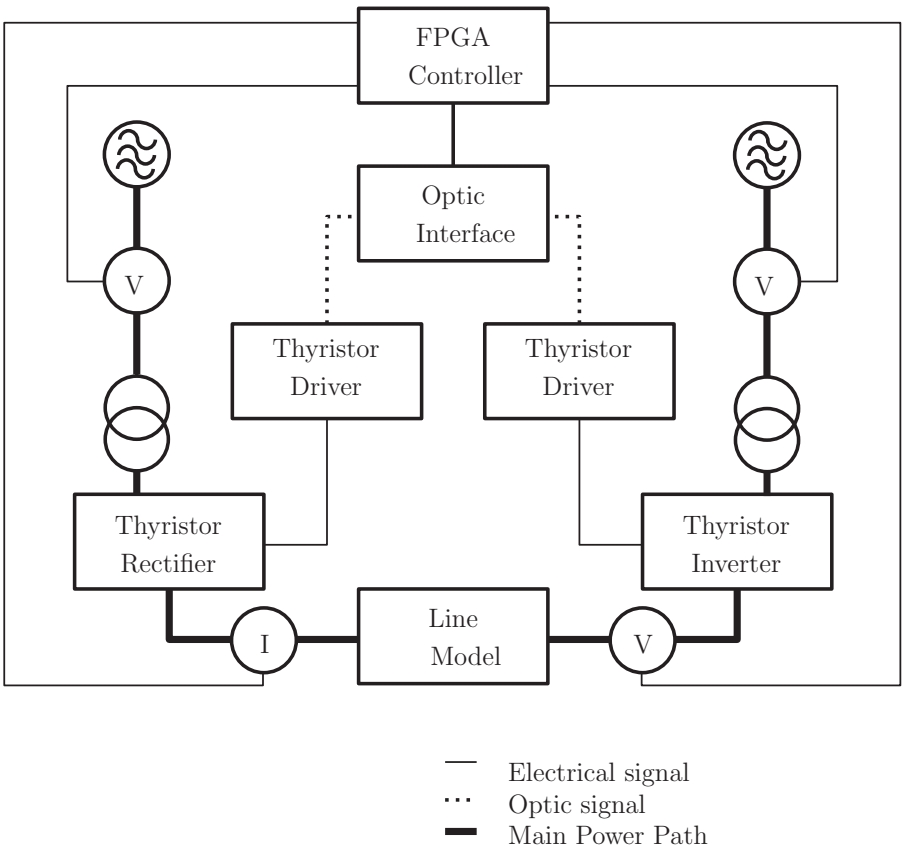

Figure 3.12 – Hardware Setup

3.4.2 Thyristor Bridge Design

The configuration of the thyristor bridge depends on the function that the converter will perform. The polarity of the thyristors are determined by the function of the converter. The thyristors in the rectifier will be connected with the cathode connected to positive side of the DC voltage. In a similar manner, the thyristors in the inverter will be connected with cathodes connected to the negative side if the DC voltage. Figure 3.13 shows the configuration of the rectifier and Figure 3.14 shows the configuration of the inverter.

Figure 3.13 and Figure 3.14 shows the schematic of a single thyristor bridge. Note that the thyristor converter is of the 12-pulse type. The thyristors are numbered in the order that they are fired. The label P indicates the positive terminal and the label N indicates the negative terminal of the thyristor converter. All the supply voltages have the same magnitude. The top and bottom three supply voltages each form a set of positive-sequence three-phase voltages. The bottom set of three-phase voltages lags the top set of three-phase voltages by 30°.

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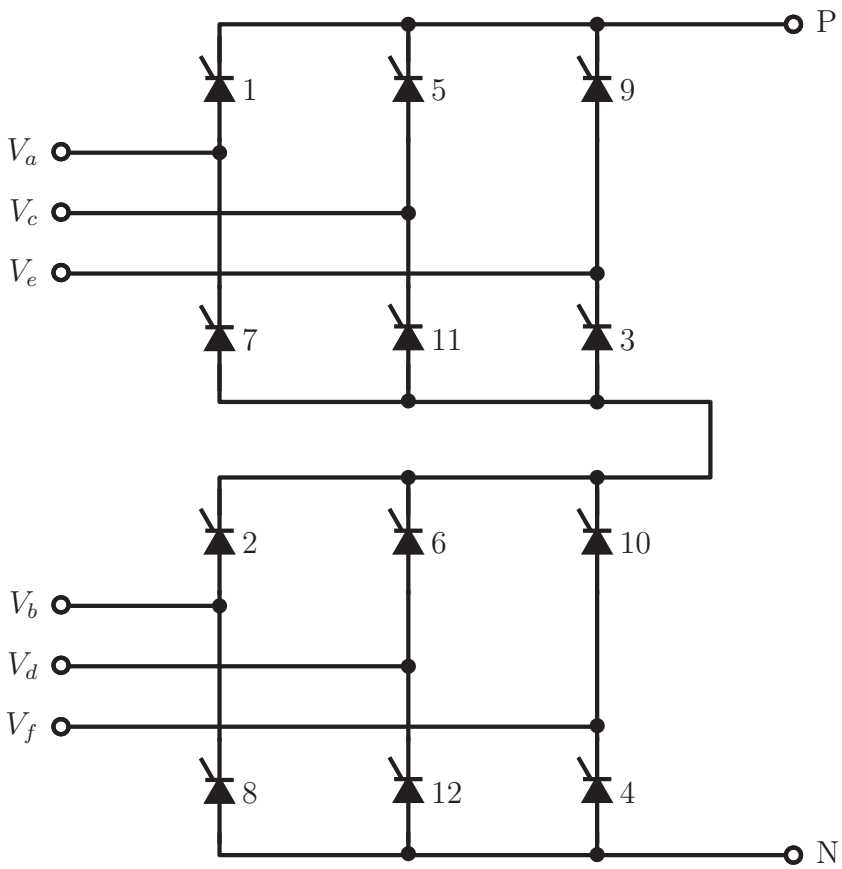

Figure 3.13 – Thyristor Bridge Schematic - Rectifier

Selection of thyristors with appropriate properties according to the required specifications will ensure safe and reliable operation. The properties that need to be considered are listed subsequently:

Latching Current (I_L) - The latching current of a thyristor is the minimum anode current that will hold the device in its on-state at the end of a triggering pulse with a duration of 10μs [42].

Holding Current (I_H) - The holding current of a thyristor is the minimum anode current that hold the device in its on-state at a temperature of 25° [42].

Circuit commutated turn-off time (t_q) - The circuit commutated turn-off time is the time the thyristor requires to discharge before it can again take on a forward voltage [42].

Critical rate of rise of on-state current ($\frac{\mathrm{d}i}{\mathrm{d}t\,cr}$) - Critical rate of rise of on-state current is the maximum change in current once the thyristor has triggered. This is due to the fact that immediately after a thyristor has triggered, only part of the chip conduct the current. Therefore the rate of current rise must be limited [42].

Critical rate of rise of off-state voltage ($\frac{\mathrm{d}v}{\mathrm{d}t\,cr}$) - The critical rate of rise off-state voltage is the maximum rate of change of the voltage across the device during its off-state. Should the maximum rate of change be exceeded, the thyristor can self trigger [42].

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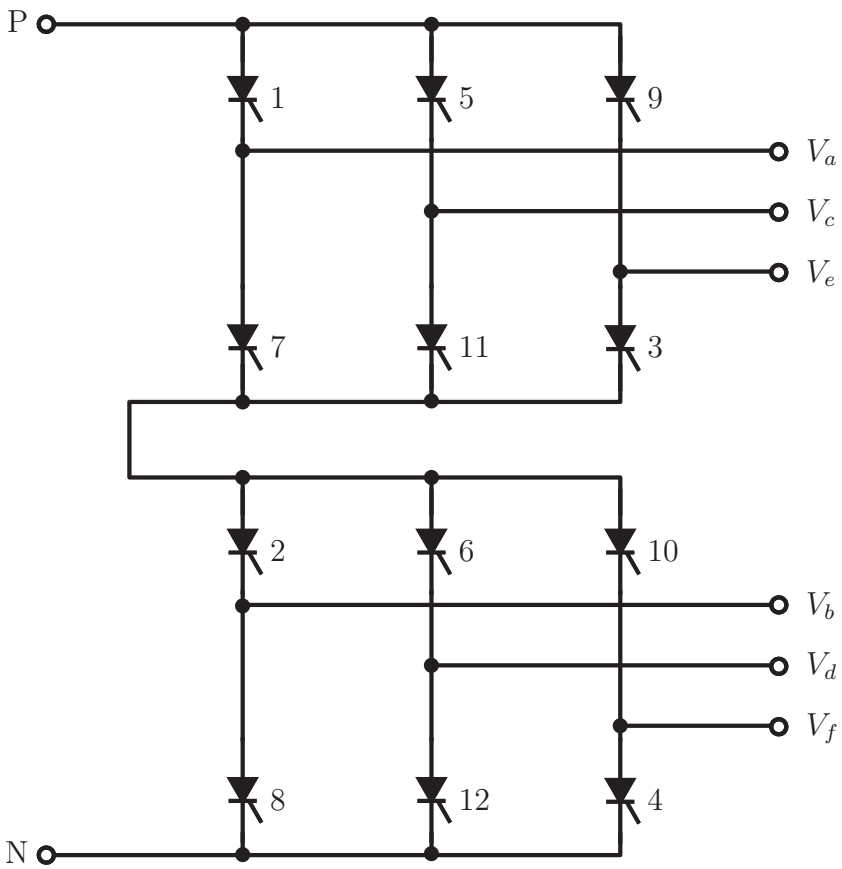

Figure 3.14 – Thyristor Bridge Schematic - Inverter

The required specifications of the components were determined with the system level simulation in Section 3.3.4. The results of the component specifications are shown in Table 3.4.

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The SKKT 57 18 E thyristor units from Semikron [43] are considered for the construction of the thyristor bridges. In Table 3.4 compares the properties of the thyristor with the required value obtained from the system level simulation done in Section 3.3.4. The first column shows the property being compared to the simulated value. The second column contains the property of the specific device that were obtained from the datasheet and the third column shows the value obtained from the simulation. The voltage rating in Table 3.4 refers both to the maximum forward blocking and maximum reverse blocking voltage.

Property	Rated	Simulated
Voltage rating	1 800 V	600 V
Current rating	57 A	3 A
I_L	0.6 A	2.96 A
I_H	0.25 A	2.96 A
t_q	80 μs	13.3 ms
$\frac{\mathrm{d}i}{\mathrm{d}t\,cr}$	150 A/μs	3 A/μs
$\frac{\mathrm{d}v}{\mathrm{d}t\,cr}$	1000 V/μs	200 V/μs

Table 3.4 – Thyristor Properties

The SKKT 57 18 E thyristor meets the required specifications and will be used for the construction of the thyristor bridges. The SKKT 57 18 E thyristor units are housed in a package referred to as Semipack 1. This package has several characteristics that provides advantages. These advantages are that there are two thyristors per package, a wide isolated base plate and bolt-on connections. Figure 3.15 shows a single Semipack 1 unit.

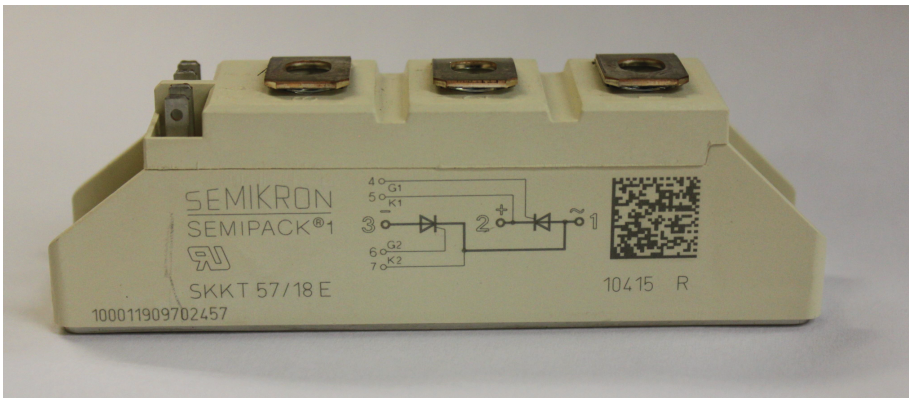

Figure 3.15 – A single Semipack 1 unit

The fact that there are two thyristors per package allows the components compact construction in comparison to what a single thyristor per package would have allowed. Compact construction avoids the use of extra heat sink or alternatively an unnecessary large single heat sink. This would keep construction costs low.

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The wide isolated baseplate gives the thyristors a lower thermal resistance. Consequently, a smaller heat sink can be used and there is no need for extra isolation that would have inhibited heat transfer.

Bolt-on connections allow the used of busbars. Bolt-on connections also allow easier replacement of damaged devices because the connections is solder free. Another advantage is that the same bolt-on connection can be used to join the thyristor terminals, busbars, cable terminations and snubber connections.

In Figure 3.16, the complete thyristor bridge is shown, complete with snubbers and the thyristor drivers. The design of the snubbers will be discussed in Section 3.4.4. These devices' design and the thermal design of the thyristor bridges will be discussed in the following sections.

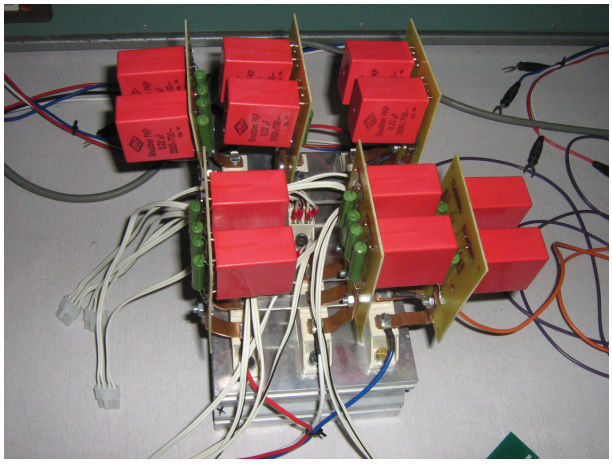

Figure 3.16 – Assembled Thyristor Bridge

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3.4.3 Thyristor Losses & Thermal Design

The loss associated with a single thyristor is given by the product of the forward voltage drop and the current flowing from the anode to the cathode. The average current through each thyristor is measured in the system level simulation to be 1 A. The forward voltage of the thyristor is given in the datasheet as 1 V [43]. Therefore the loss per thyristor is 1 W.

The used thermal design process is discussed in [44]. The thermal design for the thyristor rectifier and thyristor inverter is exactly the same. Figure 3.17 shows the equivalent schematic for a single thyristor converter. The thermal design ensures that the heat generated by the thyristors can successfully be dissipated by the heat sink without damage to the thyristors. The junction-case thermal resistance (θ_{j-c}) is given in the thyristor datasheet. The SEU16 heat sink from Semikron is used for construction. Using the datasheet [45], the sink-ambient thermal resistance (θ_{s-a}) is determined to be 0.4 K/W. The case-sink thermal resistance is approximated to be 0.2 K/W. These values are summarised in Table 3.5.

P_{loss}	1 W	Power loss per thyristor
$T_{j(max)}$	120 °C	Junction Temperature
T_{amb}	30 °C	Ambient Temperature
θ_{j-c}	0.57 K/W	Thermal resistance between junction and case
θ_{c-s}	0.2 K/W	Thermal resistance between case and sink
θ_{s-a}	0.4 K/W	Thermal resistance between sink and ambient

Table 3.5 – Thyristor Properties

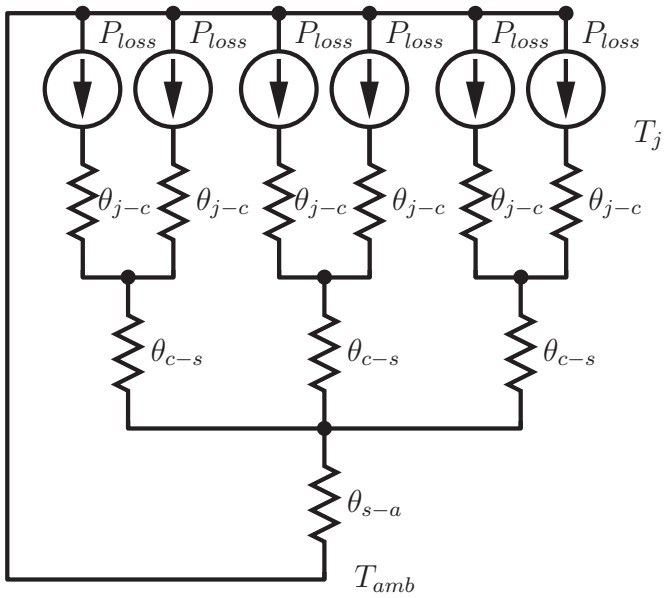

Figure 3.17 – Equivalent Thermal Circuit

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Using Figure 3.17 and assuming the ambient temperature is 30°,the operating junction temperature (T_j) is calculated to be 33.37°. It is less than the maximum junction temperature ($T_{j(max)}$) of 120°. Therefore the heat sink considered for construction is adequate.

3.4.4 Thyristor Snubbers

Snubbers are circuits connected in parallel with thyristors and other semiconductors devices used as switches to protect these devices. Snubbers used for thyristors protect them from over voltages caused by reverse recovery current and sudden changes in voltages over the device. The design procedure for a R-C snubber described in Semikron's application note will be followed [46]. A snubber circuit is designed for both six-pulse thyristor converters of both the rectifier and inverter. Therefore four snubber circuits will be designed.

Figure 3.18 shows the circuit diagram for a single thyristor. The first step is to determine the recovered charge (Q_{rr}). The datasheet of the SKKT 57 18 E thyristor shows a graph where the recovered charge is plotted against current decrease. There are curves plotted for several peak on-state currents (I_{TM}). The 5 A curve is selected because it is the closest to the simulated peak on-state current of 3 A. The current decrease is chosen as 3 A/μs based on the simulation. According to the graph, the recovered charge is given as $Q_{rr} = 100\,\mu$C.

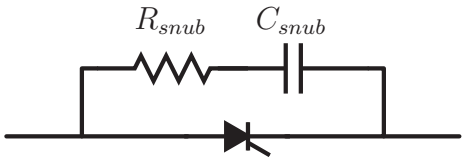

Figure 3.18 – Snubber Schematic

The snubber capacitance (C_{snub}) can now be calculated using the recovered charge in μC. Equation 3.4.1 shows the equation for the snubber capacitance with V_v defined as the maximum terminal voltage in volts.

$$C_{snub} = \frac{Q_{rr}}{V_v\sqrt{2}} \tag{3.4.1}$$

The maximum terminal voltage on the rectifier bridge is $V_{v(rec)} = 365\,\text{V}$ and on the inverter bridge $V_{v(inv)} = 272\,\text{V}$. By substituting these values into Equation 3.4.1 the snubber capacitances for rectifier and inverter is calculated. The results are shown in Equations 3.4.2 and 3.4.3.

$$\begin{aligned} C_{snub(rec)} &= \frac{Q_{rr}}{V_{v(rec)}\sqrt{2}} \\ &= 0.19\,\mu\text{F} \end{aligned} \tag{3.4.2}$$

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$$C_{snub(inv)} = \frac{Q_{rr}}{V_{v(inv)}\sqrt{2}} = 0.26\,\mu\text{F} \tag{3.4.3}$$

The closest standard capacitor value with 10 % tolerances will be used to construct the snubbers. Because the calculated values are close, a single capacitor value will be chosen to save costs. Therefore $C_{snub(rec)} = C_{snub(inv)} = C_{snub}$ and C_{snub} will be chosen as $0.22\,\mu$F.

The snubber resistance (R_{snub}) is calculated in ohms using Equation 3.4.4. The total series inductance in the circuit (L_{series}) is assumed to be dominated the leakage inductance of the transformers. The leakage inductances of the different transformers were calculated in Section 3.3.3

$$R_{snub} = \sqrt{\frac{L_{series}}{C_{snub}}} \tag{3.4.4}$$

The thyristor snubbers connected to the star-to-star connected three phase transformer will have different snubber resistances than the thyristor snubbers connected to the delta-to-star connected three phase transformer because of the different leakage inductances of the different transformers associated with each transformer bridge. The snubber resistance of the thyristor snubbers connected to the delta-to-star bridges will be denoted as R_{snub1}. Similarly, the snubber resistance of the thyristor snubbers connected to the star-to-star bridges will be denoted as R_{snub2}. Because the snubber capacitance is the same for both the rectifier and inverter the snubber resistances will also be the same.

The snubber resistance R_{snub1} is calculated in Equation 3.4.5 with $L_{series1} = 9.404\,\text{mH}$. Similarly, the snubber resistance R_{snub2} is calculated in Equation 3.4.6 with $L_{series2} = 3.889\,\text{mH}$.

$$R_{snub1} = \sqrt{\frac{L_{series1}}{C_{snub}}} = 216.84\,\Omega \tag{3.4.5}$$

$$R_{snub2} = \sqrt{\frac{L_{series2}}{C_{snub}}} = 139.45\,\Omega \tag{3.4.6}$$

According to the available standard values for 5 % resistances, R_{snub1} will be $200\,\Omega$ and R_{snub2} will be $130\,\Omega$.

The assembled snubbers mounted on the thyristors can be seen in Figure 3.16.

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3.4.5 Thyristor Gate Driver

To fire a thyristor, a current pulse of sufficient amplitude and duration through its gate and cathode is required. After the pulse has been removed, the thyristor will stay on. To ensure that the thyristor does not switch off unexpectedly, current pulses are applied to the thyristor throughout the entire on-time of the thyristor. The thyristor driver circuit provides these current pulses.The current pulses has a duty cycle of 0.3 and are applied at 20 kHz. This circuit is shown in [47]. Once, the current through the thyristor becomes zero, the thyristor will switch off.

For this application, another requirement of the driver circuit is also to provide isolation between the driver circuit and the thyristors.

Figure 3.19 shows the circuit used to drive the thyristor gate. The function of each component is explained subsequently. The component values are shown in Table 3.6.

Q_1 & R_1 - Acts a logic inverter. The transistor inverts the digital signal received from the optic fibre receiver.
Q_2 - This transistor allows current to flow though the primary of pulse transformer T_1 and the LED D_2
D_1 & Z_1 - These diodes demagnetizes the transformer when Q_2 switches off.
D_2 & R_2 - This diode is a LED and indicates whether the thyristor is being fired.
D_G - The gate diode prevents and current from the thyristor flowing into the driver circuit.
R_G - The gate resistor provides the required voltage drop from the 5 V signal to the on voltage of the thyristor.
T_1 - The pulse transformer provides the required isolation between the driver circuit and the thyristor.
R_3 - This resistor limits the current through the primary of the pulse transformer to avoid damage.

R_1	12 Ω
R_2	12 Ω
R_3	4 Ω
R_G	2.2 Ω
D_1	3 Ω
D_2	HS1A
D_G	HS1A
Z_1	MMSZ4711T1G
Q_1	MMBT2222
Q_2	BS170
T_1	TI/108 020

Table 3.6 – Thyristor Driver Component Values

Figure 3.20 a single assembled thyristor driver board. The thyristor rectifier and thyristor inverter will each require such a board.

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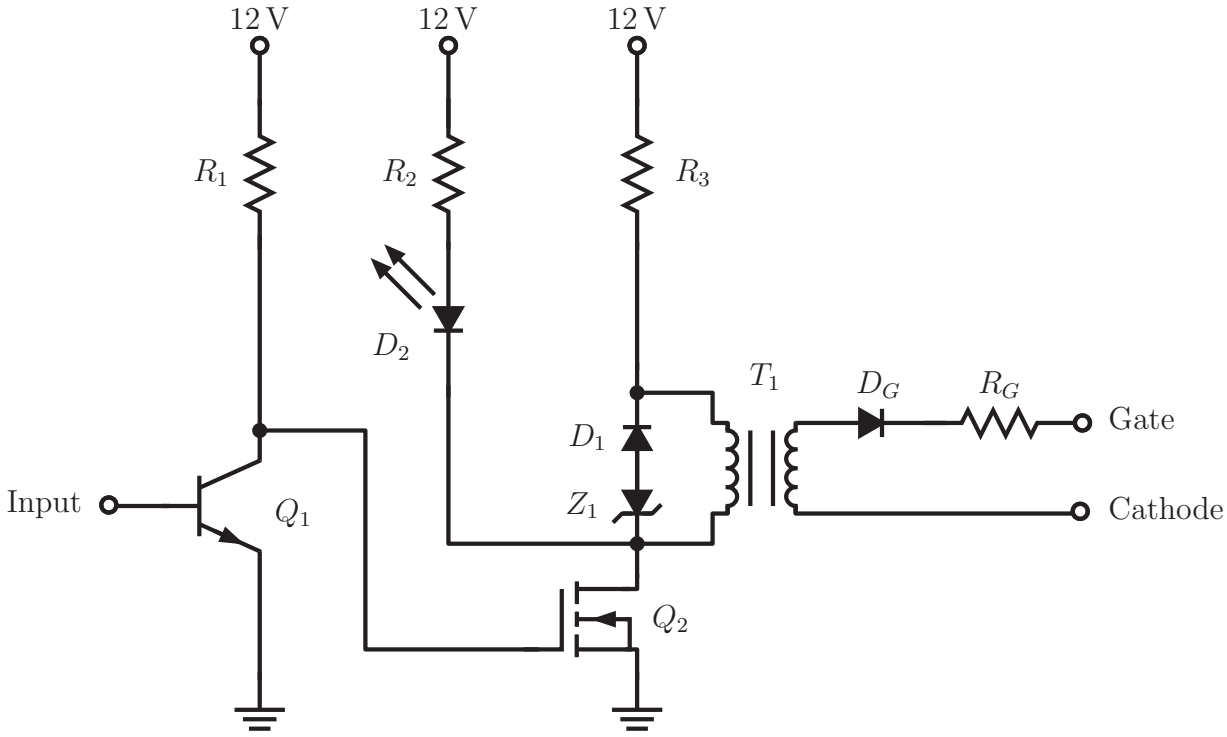

Figure 3.19 – Thyristor Driver Schematic

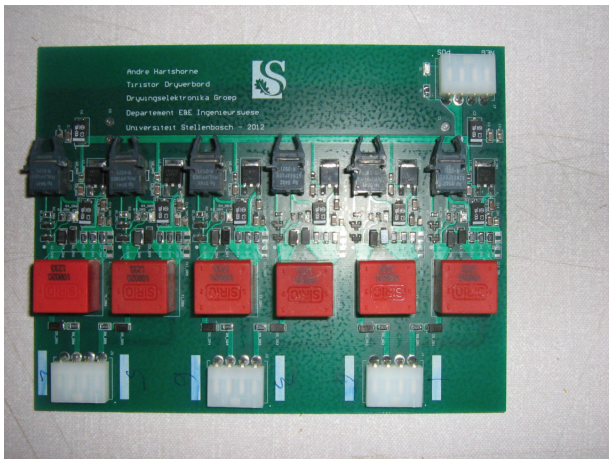

Figure 3.20 – Thyristor Driver assembled

3.4.6 Smoothing Reactor Design

The smoothing reactor is a large inductor used to smooth the line current and filter out current harmonics.

Normally, air-core inductors are used to perform this task. In an outdoor situation this is practically feasible because the magnetic and electric fields created does not affect any other equipment. In a laboratory environment, interference is an obstacle. Therefore it was decided to use an iron-core inductor. The iron-core contains most of the magnetic flux and so doing prevents most interference. The EI240 Silicon steel laminations from AMC cores were used to construct the smoothing reactors.

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During the design, it is assumed that all the flux is contained within the core and that fringing does not occur.

The design process followed for the inductor is described in [48]. Figure 3.21 shows the core that the design process is used for. The equivalent magnetic circuit is shown in Figure 3.22. The design equations will then be adapted for the shape of the core used in this project. The equivalent magnetic circuit is used to determine the equations. The magnetic reluctances ($\mathcal{R}$) are represented by resistors, the magnetic flux (ϕ) is represented by the current in the circuit and the magnetomotive force ($\mathcal{F}$) is the product of the current (i) and the number of turns (n).

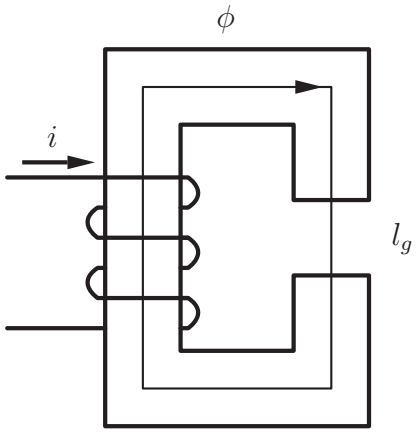

Figure 3.21 – Single leg core

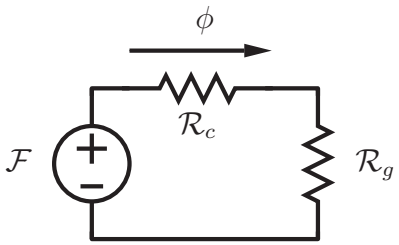

Figure 3.22 – Equivalent Magnetic Circuit

The reluctance of the core ($\mathcal{R}_c$) is assumed to be significantly smaller than the reluctance of the air gap ($\mathcal{R}_g$). This is assumed because the magnetic permeability of the iron-core is significantly higher than that of air, as shown in Equation 3.4.7. To simplify the design, the reluctance of the core will be ignored, as indicated in Equation 3.4.8

$$\mathcal{R}_c \ll \mathcal{R}_g \tag{3.4.7}$$

$$\Rightarrow \mathcal{R}_c \approx 0 \tag{3.4.8}$$

Equation 3.4.9 shows the equation to calculate the reluctance of the air gap with l_g the length of the air gap, μ_0 the magnetic permeability of free space and A_c as the cross-sectional area of the core.

$$\mathcal{R}_g = \frac{l_g}{\mu_0 A_c} \tag{3.4.9}$$

Equation 3.4.10 relates the different entities in the magnetic circuit shown in Figure 3.22.

$$\mathcal{F} = \phi \mathcal{R}_g \tag{3.4.10}$$

$$ni = \phi \mathcal{R}_g \tag{3.4.11}$$

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The maximum flux density ($B_{\max}$) specified for the core is used to calculate the maximum number of turns. The flux (ϕ) equal as the product of the flux density (B) and the cross-sectional area of the core (A_c), as shown in Equation 3.4.12.

$$\phi = BA_c \tag{3.4.12}$$

By substituting Equation 3.4.12 and Equation 3.4.9 into Equation 3.4.11 and $i_{\max}$ for i, $B_{\max}$ for B, the maximum flux density can be calculated. The result is shown in Equation 3.4.13.

$$ni_{\max} = B_{\max}A_c\mathcal{R}_g \tag{3.4.13}$$

The inductance (L) for a number of windings is given by Equation 3.4.14.

$$L = \frac{n^2}{\mathcal{R}_g} \tag{3.4.14}$$

The derived equations will now be adapted for use with an E-shaped core. Figure 3.23 shows the physical shape of the core and Figure 3.24 shows the magnetic equivalent circuit. It is important to note that the cross-sectional area of the two outer legs are equal and that the cross-sectional of each outer leg is half the cross-sectional surface area of the centre leg. These properties are mathematically described in Equations 3.4.16 and 3.4.15. The reluctances $\mathcal{R}_1$ and $\mathcal{R}_2$ can be expressed in terms of $\mathcal{R}_3$, as shown in Equation 3.4.17

$$\mathcal{R}_3 = \frac{l_g}{\mu_0 A_c} \tag{3.4.15}$$

$$\begin{aligned}\mathcal{R}_1 = \mathcal{R}_2 &= \frac{l_g}{\mu_0 \frac{1}{2} A_c} \\ &= \frac{2l_g}{\mu_0 A_c} \\ &= 2\mathcal{R}_3\end{aligned} \tag{3.4.16, 3.4.17}$$

The total reluctance ($\mathcal{R}_{\text{total}}$) of the magnetic circuit must be calculated. The sum of the reluctances are given by Equation 3.4.18

$$\begin{aligned}\mathcal{R}_{\text{totaal}} &= \mathcal{R}_1 \| \mathcal{R}_2 + \mathcal{R}_3 \\ &= \frac{1}{2}\mathcal{R}_1 + \mathcal{R}_3 \\ &= \frac{1}{2}(2\mathcal{R}_3) + \mathcal{R}_3 \\ &= 2\mathcal{R}_3 \\ &= \frac{2l_g}{\mu_0 A_c}\end{aligned} \tag{3.4.18}$$

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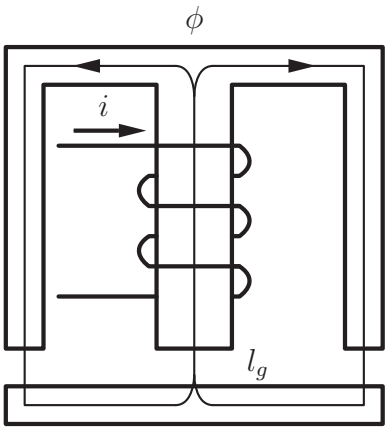

Figure 3.23 – Double Leg Core

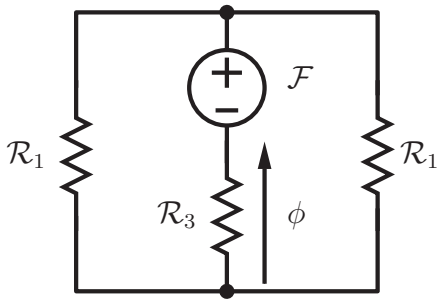

Figure 3.24 – Equivalent Magnetic Circuit Double

The total reluctance ($\mathcal{R}_{\text{total}}$) is then substituted into Equation 3.4.19 to obtained the equation for the maximum flux density ($B_{\max}$) for an E core. Equation 3.4.20 shows the result.

$$\begin{aligned} ni_{\max} &= B_{\max} A_c \mathcal{R}_{total} \\ B_{\max} &= \frac{\mu_o n i_{\max}}{2l_g} \end{aligned} \tag{3.4.19}$$

The total reluctance ($\mathcal{R}_{\text{total}}$) is then substituted into Equation 3.4.14 to obtained the equation for the inductance (L) for an E core. Equation 3.4.20 shows the result.

$$\begin{aligned} L &= \frac{n^2}{\mathcal{R}_{\text{total}}} \\ &= \frac{n^2}{\frac{2l_g}{\mu_0 A_c}} \\ &= \frac{\mu_0 n^2 A_c}{2l_g} \end{aligned} \tag{3.4.20}$$

Equation 3.4.20 will be used to calculate the number of winding (n) required to achieve the specific inductance. The inductance of the smoothing reactor is given as 0.83 H in [32].

Two design choices are made at the start of the design. The first choice is the length of the air gap. The air gap is chosen according to available materials so that a accurate air gap can easily be achieved. The air gap is chosen as $l_g = 2\,\text{mm}$. The second design choice is the maximum flux density $B_{\max}$. The maximum flux density is specified for the chosen material is 1.2 T in [49].

Figure 3.25 shows a diagram of the dimensions of the core. The laminations are stacked to a width of 120 mm. The cross-sectional area of the core can be calculated as $A_c = 9600\,\text{mm}^2$ from the measurements of the core indicated in Figure 3.25. All measurements indicated on Figure 3.25 is in mm.

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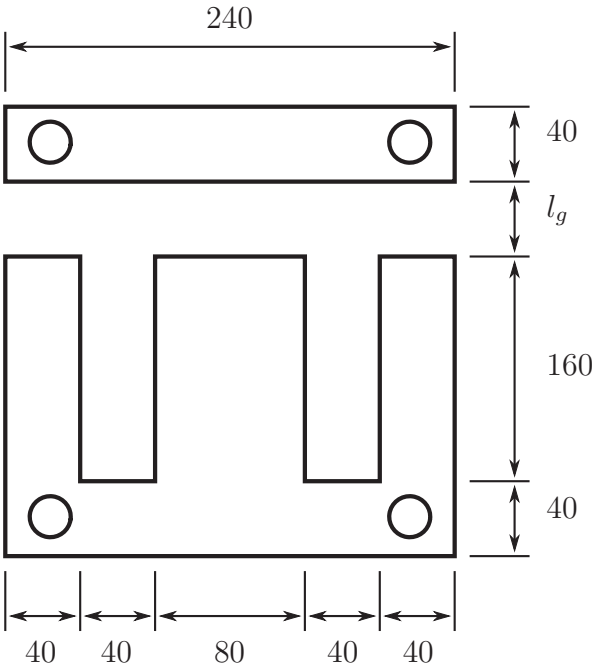

Figure 3.25 – Smoothing Reactor Core

The number of windings is calculated in Equation 3.4.21 by substituting the specified values for L, l_g and A_c.

$$n = \sqrt{\frac{2Ll_g}{\mu_0 A_c}} \tag{3.4.21}$$
$$= 524\,\text{windings}$$

(3.4.22)

The maximum magnetic flux density is then calculated using Equation 3.4.19 to ensure it does not exceed the specified maximum flux density. The result is shown in Equation 3.4.23

$$B_{\max} = \frac{\mu_o n i_{\max}}{2l_g}$$
$$= 0.49\,\text{T} \tag{3.4.23}$$

The maximum flux density that will form in the core is less than the specified maximum magnetic flux density of the material. Therefore, the calculated number of windings will not saturate the core.

The next step in the design is to see if the calculated number of windings will fit on the bobbin of the selected core. Enamel coated single strand wire with a diameter of 1.5 mm is chosen as the conductor to wound on the bobbin. The area of the bobbin that will receive the windings is referred to as the winding area. Because the wire cannot be wound without leaving spaces in between the windings, only a part of the available winding area can be used. The ratio of

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the are used by the winding to the winding area and is referred to as the fill factor. Figure 3.26 shows a typical winding area with the spaces in between the windings. All measurements indicated in Figure 3.26 is in mm.

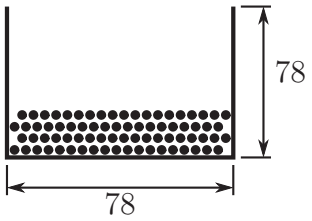

Figure 3.26 – Winding Area

For copper single strand, the fill factor is assumed to be 0.7, as mentioned in [48]. The total winding area is calculated to be 6084 mm^2, as shown in Figure 3.26. The available winding area is the product of the total winding area and the fill factor. This gives the result of an available winding area of 4259 mm^2. The area of each winding is approximated by a square with the side equal to the diameter of the wire. Therefore the approximated area of each winding is 2.25 mm^2. The available number of windings is calculated by dividing the available winding area by the area of each winding. Subsequently the available number of windings is then calculated to be 1892. Therefore the calculated required number of 524 windings will fit on the selected core.

Figure 3.27 shows one of the two assembled smoothing reactors. The inductances of the two smoothing reactors were measured after construction to ensure that accurate values were achieved.

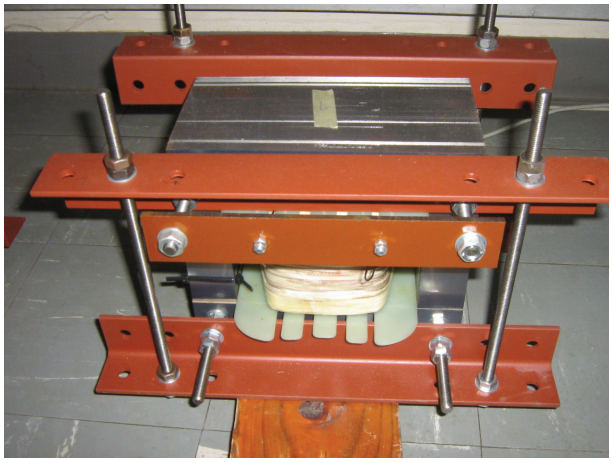

Figure 3.27 – Smoothing Reactor Assembled

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3.4.7 Line Filters

The system is studied in Chapter 2.3. The component values of the filters and the smoothing reactors were found in [32]. The component values do not need to be adapted for a lower voltage or current application because the required frequency response is independent of the used voltage or current. The topology of the filter is shown in Figure 3.28. The component values are shown in Figure 3.29.

The filter consist of a five branches. Each branch is aimed at a specific frequency. The four branches on the right are designed to filter harmonics occurring at 300 Hz, 600 Hz, 900 Hz and 1200 Hz. The branch on the left, consisting solely of capacitor C_4, acts as a high pass filter for any harmonics occurring at a higher frequencies. The capacitor C_5 forms a voltage divider with the parallel combination of the filter branches. The impedance of capacitor C_5 is higher that the impedance of the parallel combination of the filter branches. Therefore the greatest voltage drop occurs across C_5. Consequently, only C_5 will have to be of a high voltage rating and the other filter components can have lower voltage ratings, leading to cheaper filter components.

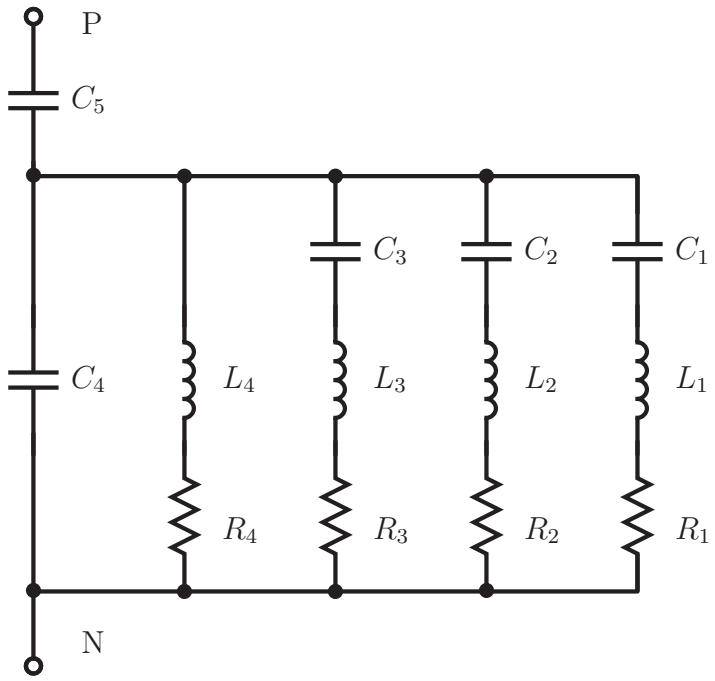

Figure 3.28 – Line Filter Schematic

C_1	0.018 μF
C_2	0.035 μF
C_3	0.13 μF
C_4	0.288 μF
C_5	0.15 μF
L_1	1.0 H
L_2	1.0 H
L_3	0.5314 H
L_4	0.236 H
R_1	12 Ω
R_2	12 Ω
R_3	6 Ω
R_4	3 Ω

Figure 3.29 – Line Filter Component Values

Figure 3.30 shows a single assembled line filter. The minimum power rating of the components were calculated using the RMS current flowing in each filter leg. These currents are determined using the system level simulation performed in Section 3.3.4.

Capacitors with low ESR were chosen to keep losses to a minimum. To achieve accurate capacitances, several capacitors were connected in parallel. Variable resistors of sufficient power rating were used to achieve accurate resistor values. Accurate inductances is achieved by adjusting the air-gap of the cores until the correct inductance were achieved. The inductors were constructed using the same methodology as discussed in Section 3.4.6.

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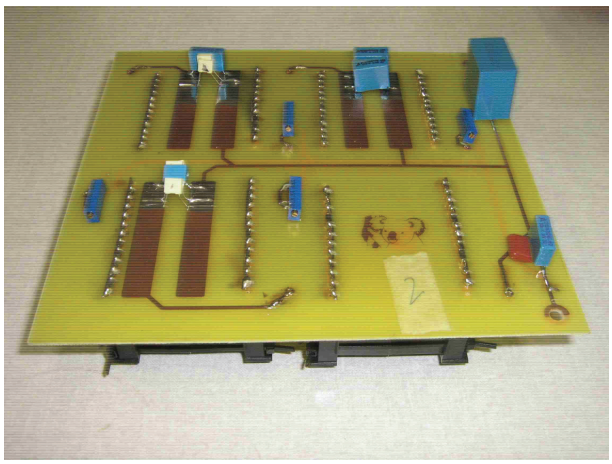

Figure 3.30 – Line Filters Assembled

3.4.8 Transformer Banks

As mentioned in Section 3.2, the converters are to be of the 12-pulse type. Therefore two set of three-phase voltages with a 30° phase differences must be supplied to the converter. Each voltage must be of the same magnitude. The 30° phase difference between the sets are created by supplying the converter with one set through a star-star connected three-phase transformer and the other set though a delta-star connected three-phase transformer. Figure 3.31 shows the schematic of transformer bank.

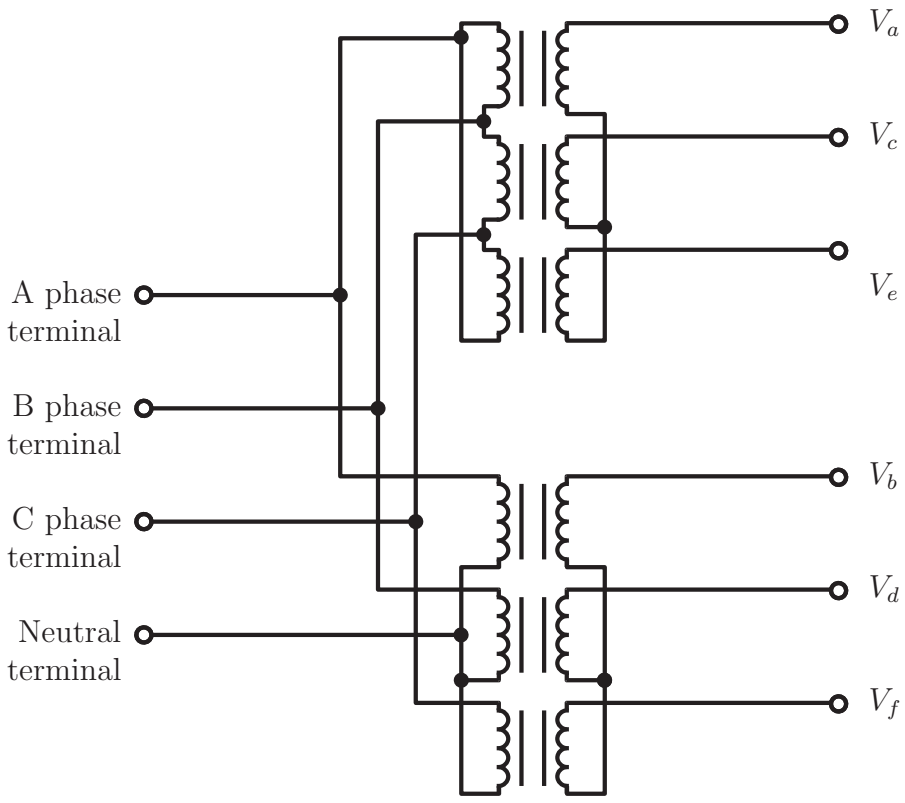

Figure 3.31 – Transformer Bank

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Individual single-phase transformers were inter-connected to form three-phase transformers. Single-phase transformers were chosen to allow for versatility for future developments. Each converter has its own transformer bridge to supply the voltages. Figure 3.32 shows one of assembled transformer banks.

Figure 3.32 – A Single Assembled Transformer Bank.

The two sets of three-phase voltages operate at different voltages in relation to ground because of the function the converter. Therefore, the neutral points of the star connections of the transformers' secondaries are allowed to be left floating.

Correct operation of the converters can only be achieved if isolation between the two sets of three-phase voltages is maintained throughout operation. The isolation of the transformers was specified at 5 kV. The isolation is chosen to ensure safe functioning of the transformers while the outputs are connected in series, even should a fault occur during operation of the HVDC Terminals Model.

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3.4.9 Controller Board

A Controller Board is required to implement the control law, generate gating signals and take measurements. A single controller board must control the rectifier and the inverter. Twenty-four thyristors have to be controlled in total. Four measurements need to be taken to implement the proposed control system. The controller board will perform all digital processing. Required processing includes gate signal generation, switch debouncing and LCD screen control. This controller board has been developed and constructed by Heinrich Fuchs.

The available Controller Board is FPGA based and will be used to control the entire setup. The Controller Board uses the Cyclone III EP3C400240C8 FPGA from Altera. A FPGA falls under the category of programmable digital logic devices. These devices allows the implementation of digital logic circuits rather than relying on DSP architectures. This allows several processes to be performed simultaneously. VHDL is used to describe the digital circuits that will be programmed on the FPGA.

The controller board has 36 digital pins that can be configured either as inputs or outputs. The controller board also has eight analog channels that use differential signals.

Figure 3.33 shows the FPGA Controller Board.

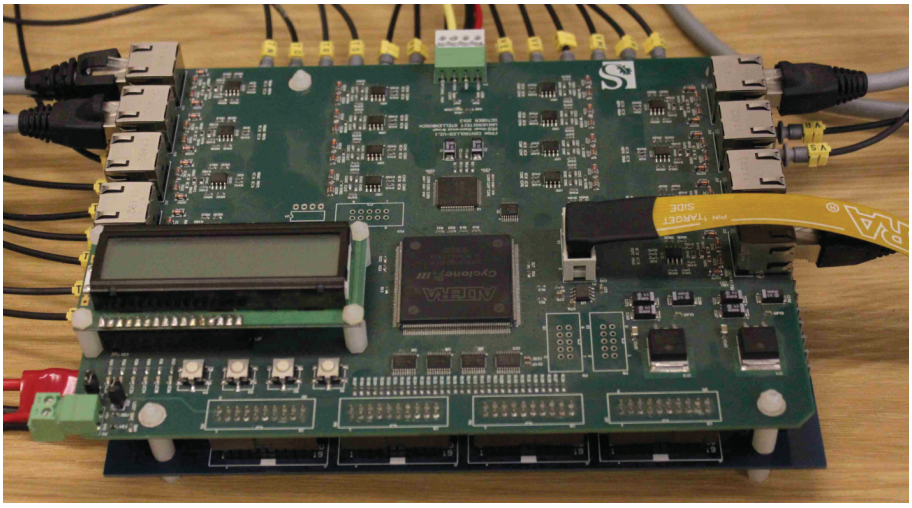

Figure 3.33 – FPGA Controller Board

3.4.10 Voltage Measurement Board

Voltages in the system is measured by the use of a voltage measurement board. Resistors perform voltage division so that a low voltage can be measured by an op-amp. The op-amp also serves as a buffer between the measurement board and the A/D converter on the FPGA converter board. Fully differential op-amps are used to generate differential signals. The THS4001 fully differential from Texas Instruments was chosen for its high bandwidth and high slew

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rate. Differential signals will reduce common mode noise. Figure 3.34 shows a picture of the assembled board. This board has been developed and constructed by Heinrich Fuchs.

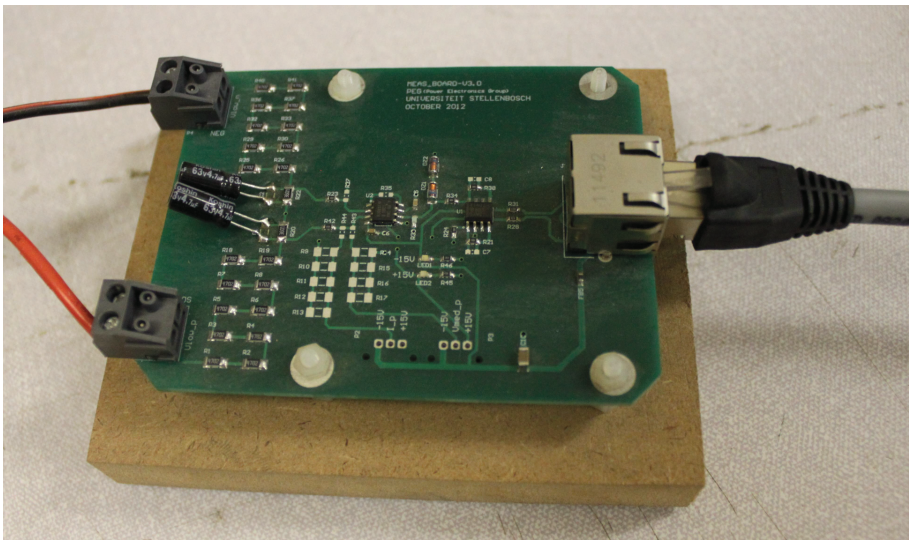

Figure 3.34 – Voltage Measurement Board

3.4.11 Current Measurement Board

Currents in the system is measured by the use of current transducers. The NTSR 6-NP from LEM is selected. The transducer provide galvanic isolation from the system, yet provide accurate readings within a specified bandwidth. Voltages signals from the current transducer is buffered using the voltage measurement board. Figure 3.35 shows a photograph of the assembled current measurement board. This board has been developed and constructed by Heinrich Fuchs.

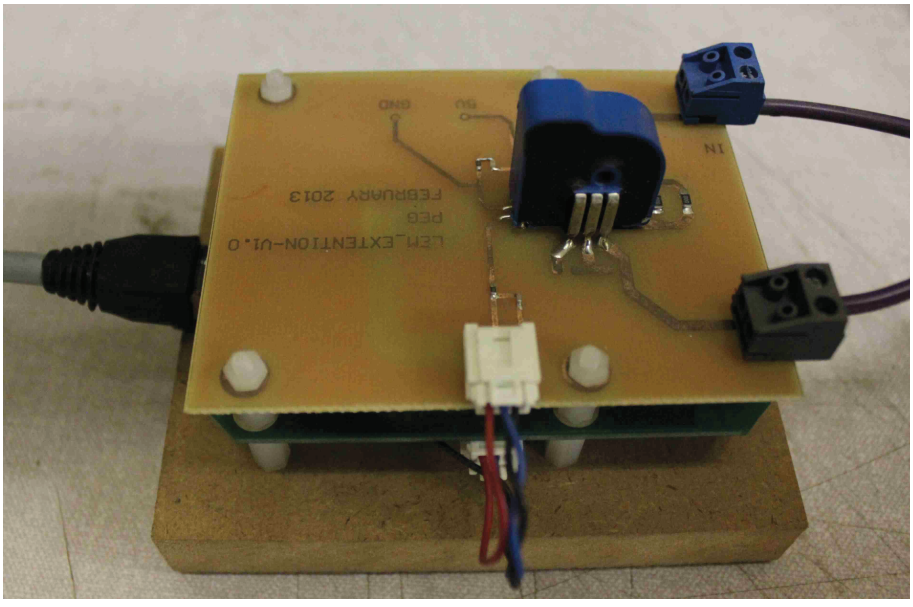

Figure 3.35 – Current Measurement Board

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3.4.12 Optic Fibre Driver Board

The gate signals of the thyristor rectifier and thyristor inverter will be transmitted with optic signals, as shown in Figure 3.1. A optic fibre driver board will be required to convert the digital gate signals from the controller board to optic signals and transmit them to the thyristor driver circuits. Such a optic fibre driver board is already available. Figure 3.36 shows the optic fibre driver board used to drive the optic fibres. This board has been developed and constructed by Males Tomlinson.

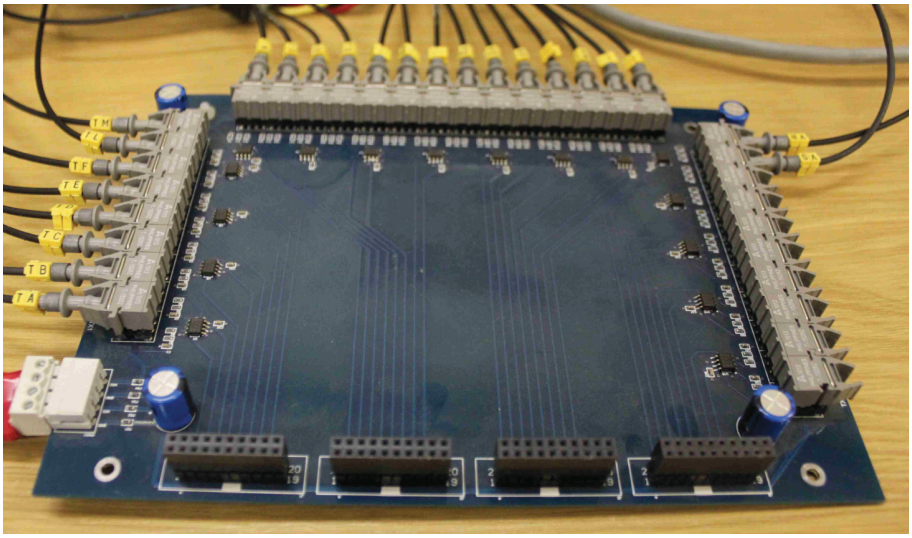

Figure 3.36 – Optic Fibre Driver Board

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3.5 Results

Figure 3.37 shows the practical setup of the HVDC Terminals model. The rectifier converter is on the left and the inverter converter is on the right.

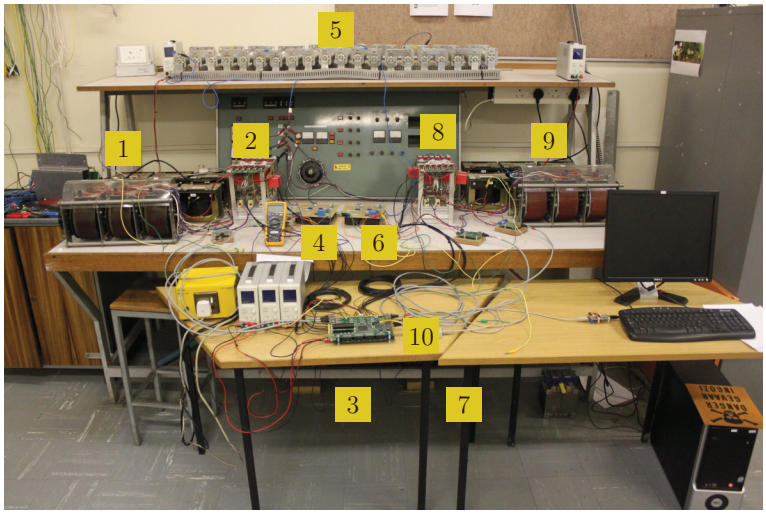

Figure 3.37 – Practical Setup

Table 3.7 gives the legend of the different components.

1	Rectifier Transformer Bank
2	Complete Thyristor Rectifier
3	Rectifier Smoothing Reactor
4	Rectifier Line Filter
5	Line Resistance
6	Inverter Line Filter
7	Inverter Smoothing Reactor
8	Complete Thyristor Inverter
9	Inverter Transformer Bank
10	Controller

Table 3.7 – Practical Setup Legend

Several measurements were taken to compare with simulation waveforms to ensure that the practical systems act as simulated. The voltages V_{DCrec} and V_{DCinv} were measured and is shown in Figures 3.38 and Figure 3.39. The line current I_{line} was also measured and is shown in Figure 3.40. The fire angle of the rectifier was set at 30° and the fire angle of the inverter set at 150°. Figure 3.1 shows the definitions of the voltages and current.

As shown in Figures 3.38 and 3.39, each voltage V_{DCrec} and V_{DCinv} has the same mean value as simulated in Section 3.3.4, although it is found that both voltages have higher harmonic content than expected. The line current shown in Figure 3.40 also has the same mean value as simulated, although a larger ripple current is present. The difference in simulated and practical measurements is ascribed to non-idealities present in the practical system that was not modelled in the simulation, for example noise present on the supply voltages.

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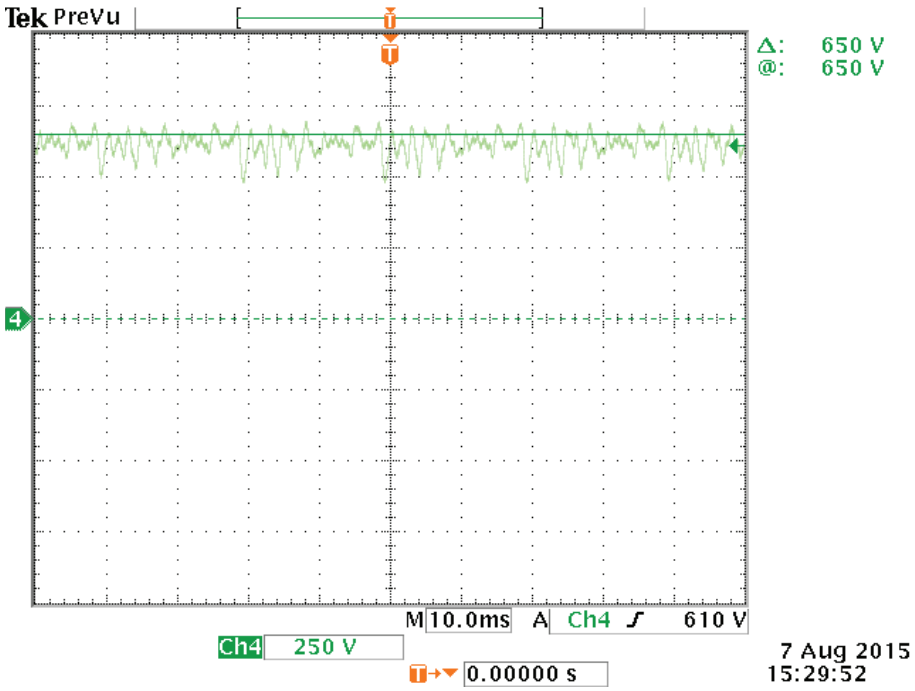

Figure 3.38 – Measured V_{DCrec}

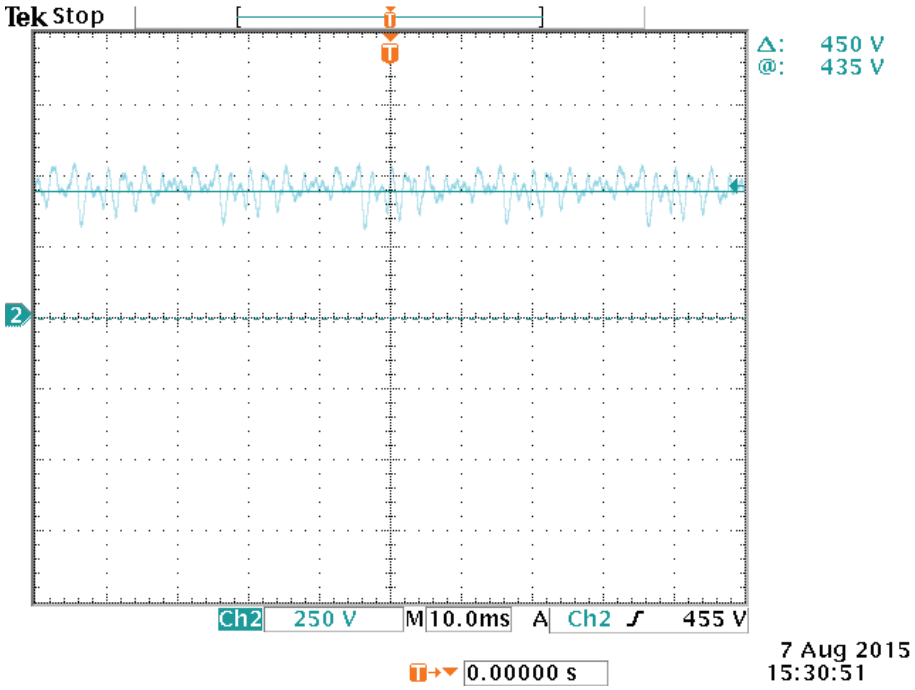

Figure 3.39 – Measured V_{DCinv}

The practical measurements show that the construction of HVDC Terminals model is successful, although there are more harmonic content present as originally simulated. The presence of additional harmonics will not hinder the development of the controllers of the HVDC Terminals model or the HVDC Series Tap model.

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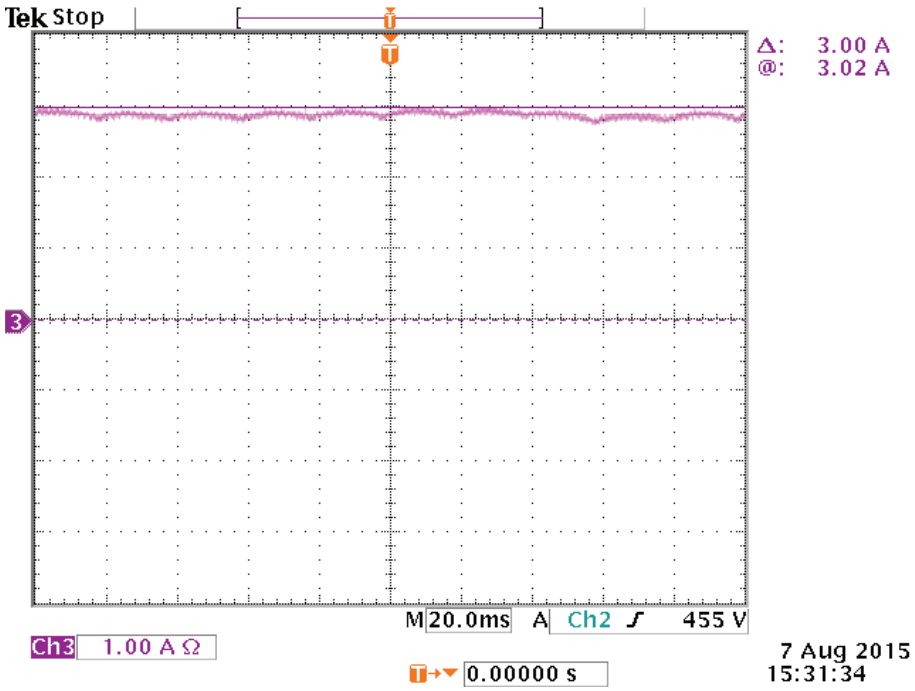

Figure 3.40 – Measured I_{line}

3.6 Summary

In this chapter the HVDC Terminals model was design and simulated at system level. Simulation results of the system level design were presented. Thereafter, the design of the hardware used to construct the HVDC Terminals model was discussed. The chapter concludes with an open-loop test of the HVDC Terminals model.

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Chapter 4

HVDC Terminals Model Controller Design

4.1 Introduction

This chapter discusses the design and implementation of the controllers of the Thyristor Rectifier and Thyristor Inverter.

In Section 3.2, the current and voltage values are specified. These values will be implemented as the reference values for the controllers. Figure 3.1 shows how the different currents and voltages are defined. Section 3.3.2 gives the formula that relates the input voltage to the output voltage of the thyristor bridge.

The control scheme that will be followed is discussed in Section 2.2.7. Therefore the rectifier will be under constant current control and the inverter will be under constant voltage control.

First the rectifier will be designed and simulated. Subsequently, the inverter will be designed and simulated. Thereafter, both controllers will be implemented in a single simulation. Next, both controllers will be implemented and measured. Lastly, a conclusion is presented.

4.2 Rectifier Controller

4.2.1 Overview

A control loop is implemented with the purpose to regulate a specific current or voltage. The plant ($G(s)$) of the system describes the transient behaviour of the system that will be controlled. The controller ($D(s)$) will perform the control function. Figure 4.1 shows a basic feedback system. The rectifier must deliver a constant current to the system to facilitate constant power transfer. The rectifier will use I_{line} as the reference.

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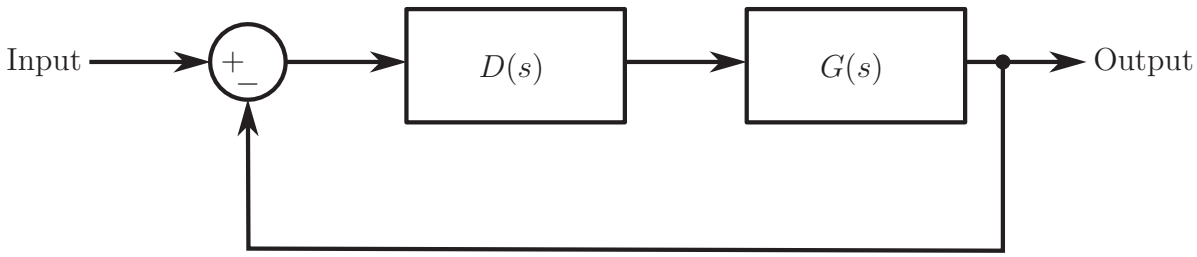

Figure 4.1 – Basic Control System

A controller must be designed according to the behaviour of the plant, in order to achieve specific closed-loop behaviour. Therefore the transfer function of the plant must be determined before the controller can be designed.

4.2.2 Determine transfer function

The line current (I_{line}) is given by Equation 4.2.1. This is achieved by summing all the voltages in the loop, with $V_{DCrec} = 2.7V_{ACrec}\cos\alpha_r$, as stated in Equation 3.3.2.

$$\begin{aligned} I_{line} &= \frac{V_{DCrec} - V_{DCinv}}{R_{line}} \\ &= \frac{2.7V_{ACrec}\cos\alpha_r - V_{DCinv}}{R_{line}} \end{aligned} \tag{4.2.1}$$

It is important to note that I_{line} is assumed to be a DC current. This assumption can be made because the dynamics of the controller is much slower than that of the line.

Equation 4.2.1 will have to be linearised around an operating point so that a control design can be performed.

Equation 4.2.1 will be linearised with a firing angle of 30 °. This firing angle was specified as the operating angle for the rectifier in Section 3.2. The $\cos(\alpha_r)$ will be approximated by a straight line with the expression $m\alpha_r + c$. The constant m will be determined by evaluating the derivative at the operating point. This is shown in Equation 4.2.2

$$\begin{aligned} m &= \frac{\mathrm{d}}{\mathrm{d}\alpha}\left(cos\alpha_r\right) \\ &= -\sin\alpha_r \end{aligned} \tag{4.2.2}$$

When the derivative is evaluated at the chosen operating point of 30°, the gradient is found to be $m = -\frac{1}{2}$.

The constant c will be determined by the evaluating $\cos(\alpha_r)$ at the operating point setting the result equal to expression $m\alpha_r + c$. This is shown in Equation 4.2.3.

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$$\begin{aligned}
\cos(\alpha_r) &= m(\alpha_r) + c \\
\cos\left(\frac{\pi}{6}\right) &= -\frac{1}{2}\left(\frac{\pi}{6}\right) + c \\
\frac{\sqrt{3}}{2} &= -\frac{1}{2}\left(\frac{\pi}{6}\right) + c \\
c &= \frac{\sqrt{3}}{2} + \frac{\pi}{12} \\
c &= 1.128
\end{aligned} \tag{4.2.3}$$

Equation 4.2.4 shows the rectifier equation with the $\cos\alpha_r$ replaced with the linearised approximation.

$$\begin{aligned}
I_{line} &= \frac{2.7V_{ACrec}(m\alpha_r + c) - V_{DCinv}}{R_{line}} \\
&= \frac{2.7(257)(-0.5\alpha_r + 1.128) - 450}{50} \\
&= -6.939\alpha_r + 6.654
\end{aligned} \tag{4.2.4}$$

4.2.3 Design of controller

According to [5], the Proportional-Integral controller (PI controller) is the most common implemented controller for HVDC thyristor converters. Therefore a PI controller will be implemented for both converters of the HVDC Terminals Model. A PI controller is generates the control signal by adding a signal proportional to the error signal and a signal proportional to the integral of the error signal. Figure 4.2 shows the block diagram of a PI controller. The values used to describe the proportion of the signals are k_p and k_i.

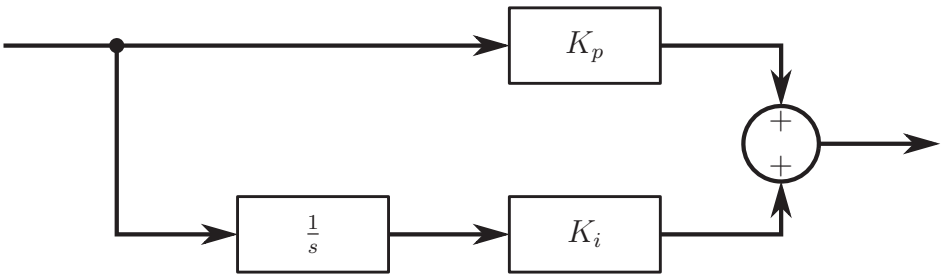

Figure 4.2 – PI Controller

The controller transfer function $D(s)$ will now be derived. Equation 4.2.5 shows the result.

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$$\begin{aligned} D(s) &= k_p + \frac{k_i}{s} \\ &= \frac{k_p s}{s} + \frac{k_i}{s} \\ &= \frac{k_p s + k_i}{s} \\ &= k_p \frac{(s + \frac{k_i}{k_p})}{s} \end{aligned} \tag{4.2.5}$$

The system error will be zero because the controller contains an integrator, even if any disturbances are present. Therefore the constant value c of the linearised equation relating the fire angle of the rectifier (α_r) to the line current (I_{line}) will be modelled as a disturbance. The transfer function that will be used for the design is given in Equation 4.3.5.

$$G_r(s) = \frac{I_{line}}{\alpha_r} = -6.939 \tag{4.2.6}$$

The bandwidth (f_{BW}) of the controller is chosen to be 5 Hz. The value of $\frac{k_i}{k_p}$ is chosen to be equal to the bandwidth. Equation 4.2.7 shows the result.

$$\begin{aligned} \frac{k_i}{k_p} &= 2\pi f_{BW} \\ &= 2\pi 5 \\ &= 31.4 \end{aligned} \tag{4.2.7}$$

The gain k_p of the controller is then increased until the acceptable step response is observed. The over-shoot must be below 0.05 of the step value. The SISO tool from Matlab will be used to design the PI controller using the root locus method. Figure 4.3 show the design screen of the SISO tool after the design has been completed.

Figure 4.4 shows the step response of the closed loop has an over-shoot of 1.045 of the step value of 1. The gain of the controller is recorded to be 3.49. According to Equation 4.2.5 the k_p value is equal to the gain. The k_i value is consequently calculated to be $k_i = 109.586$. The rectifier controller design is then confirmed in Simulink. Figure 4.6 shows the setup in Simulink used to simulate the controller.

Figure 4.5 shows the results of a step test performed in Matlab's Simulink tool. The grey trace is the output response and the black trace is the step input. The overshoot is less than 0.05 of the value of the step.

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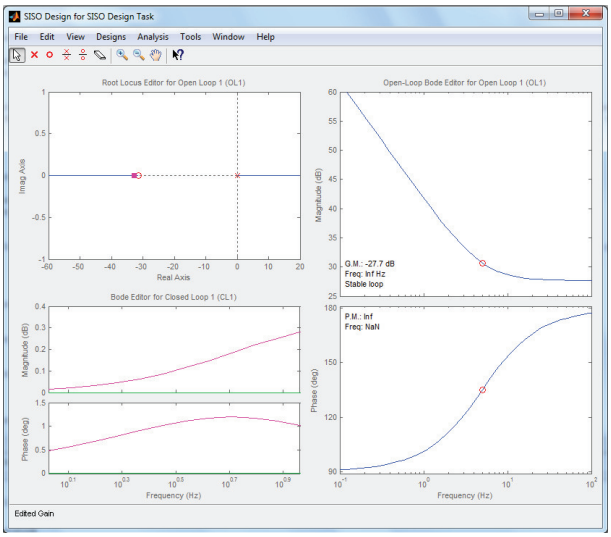

Figure 4.3 – SISO Tool Design - Rectifier

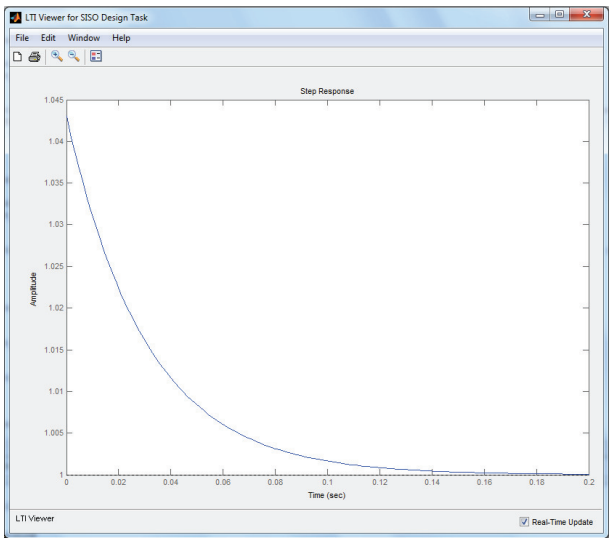

Figure 4.4 – SISO Tool Design - Rectifier Unit Step

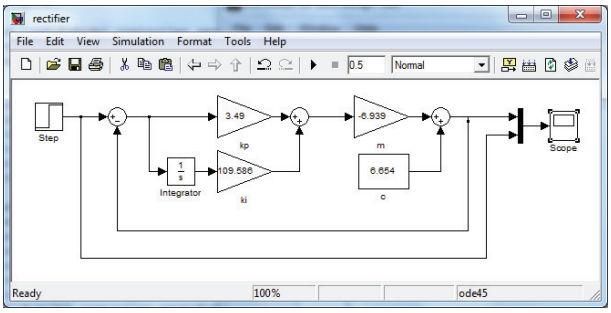

Figure 4.5 – Simulink - Setup

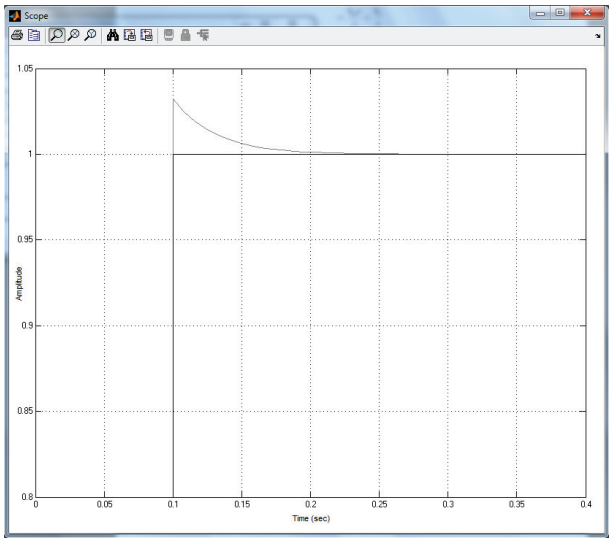

Figure 4.6 – Simulink - Step Test

4.3 Inverter Controller

4.3.1 Overview

The controller for the inverter will also be a PI-controller. The inverter must provide a constant voltage to the system to facilitate constant power transfer. The inverter will use V_{DCinv} as the reference. The transfer function of the inverter will be determined by following the same procedure used to determine the transfer function of the rectifier.

4.3.2 Determine transfer function

The transfer function for the inverter is derived from Equation 3.3.3 and is given below.

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$$\begin{aligned} V_{DCinv} &= -2\frac{3\sqrt{2}}{\pi}V_{ACinv}\cos(\alpha_i) \\ &= -2.7V_{ACinv}\cos(\alpha_i) \end{aligned} \tag{4.3.1}$$

Equation 4.3.1 will be linearised with a firing angle of 150 °. This firing angle was specified as the operating angle for the inverter in Section 3.2. The $\cos(\alpha_i)$ will be approximated by a straight line with the expression $m\alpha_i + c$. The constant m will be determined by evaluating the derivative at the operating point, as shown in Equation 4.3.2

$$\begin{aligned} m &= \frac{\mathrm{d}}{\mathrm{d}\alpha}\big(cos\alpha_i\big) \\ &= -\sin\alpha_i \end{aligned} \tag{4.3.2}$$

When the derivative is evaluated at the chosen operating point of 150°, the gradient is found to be $m = -\frac{1}{2}$.

The constant c will be determined by the evaluating $\cos(\alpha_i)$ at the operating point setting the result equal to expression $m\alpha_i + c$. This is shown in Equation 4.3.3.

$$\begin{aligned} \cos(\alpha_i) &= m(\alpha_i) + c \\ \cos\Big(\frac{5\pi}{6}\Big) &= -\frac{1}{2}\Big(\frac{5\pi}{6}\Big) + c \\ -\frac{\sqrt{3}}{2} &= -\frac{1}{2}\Big(\frac{5\pi}{6}\Big) + c \\ c &= -\frac{\sqrt{3}}{2} + \frac{5\pi}{12} \\ c &= 0.443 \end{aligned} \tag{4.3.3}$$

Equation 4.3.4 shows the inverter equation with the $\cos\alpha_i$ replaced with the linearised approximation.

$$\begin{aligned} V_{DCinv} &= -2.7V_{ACinv}(m\alpha_i + c) \\ &= -2.7(192)(-0.5\alpha_i + 0.443) \\ &= 259.2\alpha_i - 229.7 \end{aligned} \tag{4.3.4}$$

4.3.3 Design of controller

The same design method used for the rectifier will be used for the inverter. The bandwidth (f_{BW}) must also be 5 Hz. The constant c will once again be modelled as a disturbance. The transfer function for the inverter controller will also be Equation 4.2.5.

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$$G_i(s) = \frac{V_{DCinv}}{\alpha_i} = 259.2 \tag{4.3.5}$$

As stated above, the bandwidth (f_{BW}) of the controller is chosen to be 5 Hz. The value of $\frac{k_i}{k_p}$ is chosen to be equal to the bandwidth. Equation 4.3.6 shows the result.

$$\begin{aligned} \frac{k_i}{k_p} &= 2\pi f_{BW} \\ &= 2\pi 5 \\ &= 31.4 \end{aligned} \tag{4.3.6}$$

The gain k_p of the controller is then increased until the acceptable step response is observed. The settling time must be below 0.4 s. The SISO tool from Matlab will be used to design the PI controller using the root locus method. Figure 4.3 shows the design screen of the SISO tool after the design has been completed.

Figure 4.8 shows the step response of the closed loop to have a settling time of 0.2 s. The gain of the inverter controller is recorded to be 0.5. According to Equation 4.2.5 the k_p value is equal to the gain. The k_i value is consequently calculated to be $k_i = 15.7$.

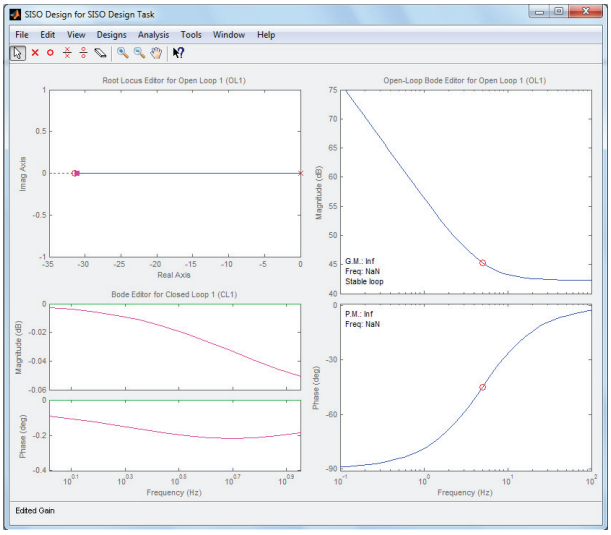

Figure 4.7 – SISO Tool Design - Inverter

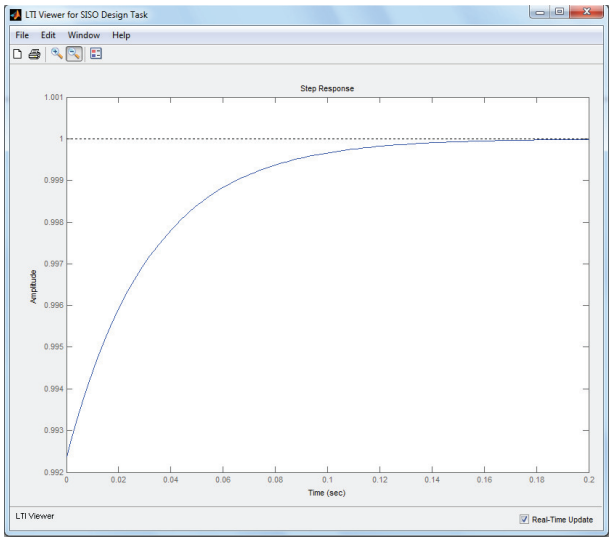

Figure 4.8 – SISO Tool Design - Inverter Unit Step

The inverter controller design is then confirmed in Simulink. Figure 4.10 shows the setup in Simulink used to simulate the controller.

Figure 4.9 shows the results of a step test performed in Matlab's Simulink tool. The grey trace is the output response and the black trace is the step input.

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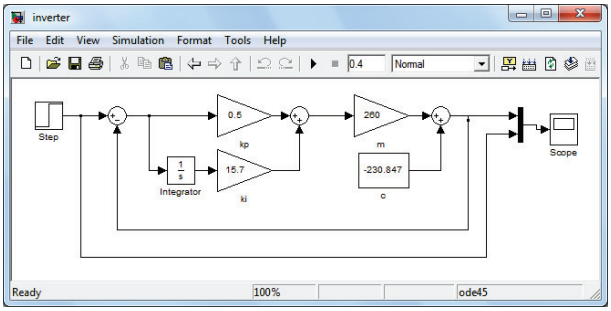

Figure 4.9 – Simulink - Setup

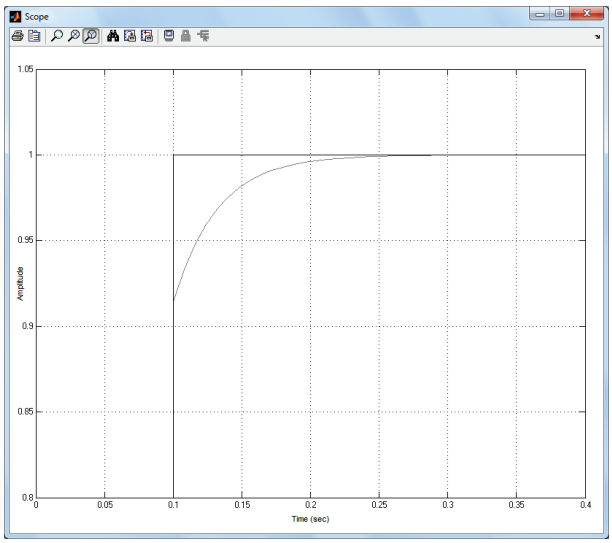

Figure 4.10 – Simulink - Step Test

4.4 System Simulation & Implementation

4.4.1 System simulation

Simplorer 15 is used to perform a system level simulation of the rectifier- and inverter controllers. Figure 4.11 shows a screenshot of the Simplorer workspace.

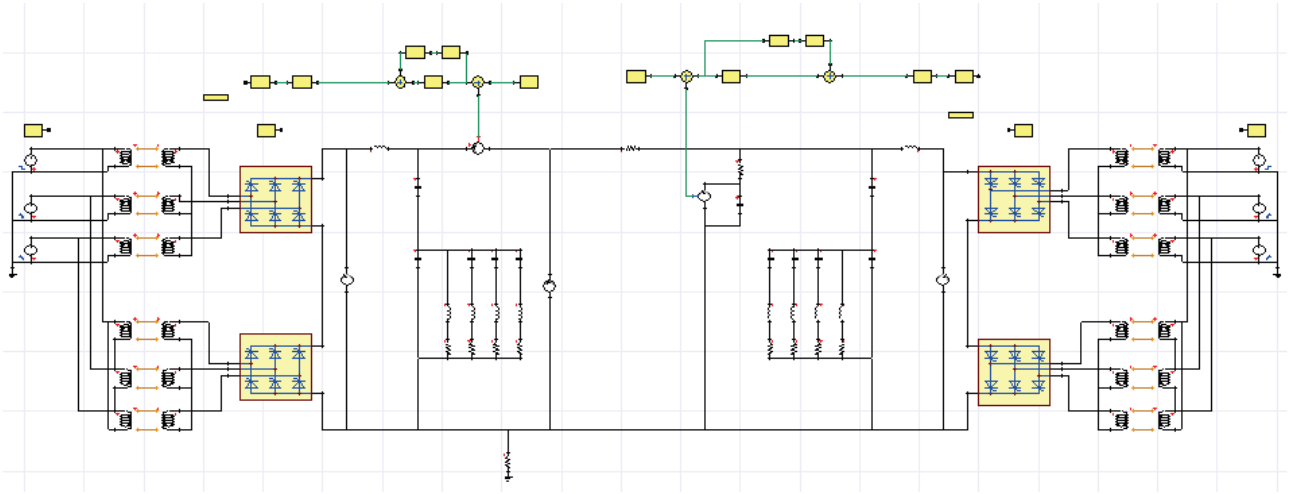

Figure 4.11 – Simplorer 15 Workspace Screenshot

Table 4.1 shows the simulation parameters. The component values are the same as described in Sections 3.4.6 and 3.4.7.

In order to prove the controllers function correctly, the supply voltages V_{ACrec} and V_{ACinv} were changed when the simulation time reached 100 ms. Figure 4.12 shows how the rectifier controller responds to a change in the supply AC voltage V_{ACrec}.

Total time	1500 ms
Minimum time step	1 μs
Maximum time step	10 μs

Table 4.1 – Simulation Parameters

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The supply voltage V_{ACrec} is changed from 365 V peak to 376 V peak. Figure 4.14 shows how the inverter controller responds to a change in the supply AC voltage V_{ACinv}. The supply voltage V_{ACinv} is changed from 270 V peak to 282 V peak.

In Figures 4.12 and 4.13, the current waveform of I_{line} are shown. The rectifier controller regulates the current and responds to the change in the supply voltage V_{ACrec}. Figures 4.14 and Figure 4.15 show the voltage waveform of V_{DCinv}. The inverter controller regulates the voltage and response to the change in the supply voltage V_{ACrec}. The inverter controller controls a voltage that forms part of the plant that the rectifier controller controls. Therefore the settling time of the inverter controller will be affected by the settling time of the rectifier controller. In this case, both controllers' settling time are observed to be 0.17 s. It is concluded that the system level simulation of both controllers is successful because both controllers' are within the respective specifications.

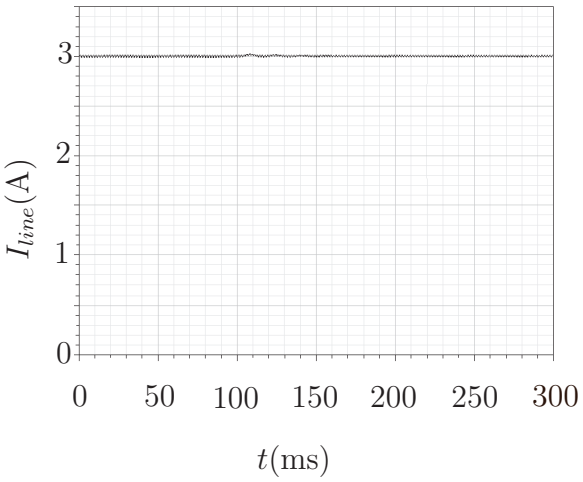

Figure 4.12 – Rectifier Control

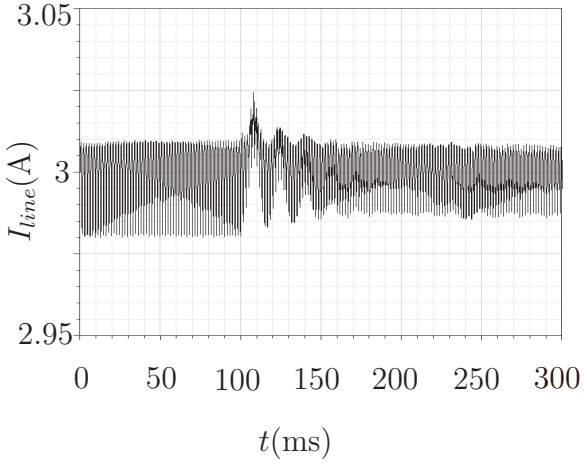

Figure 4.13 – Rectifier Control - Enlarged

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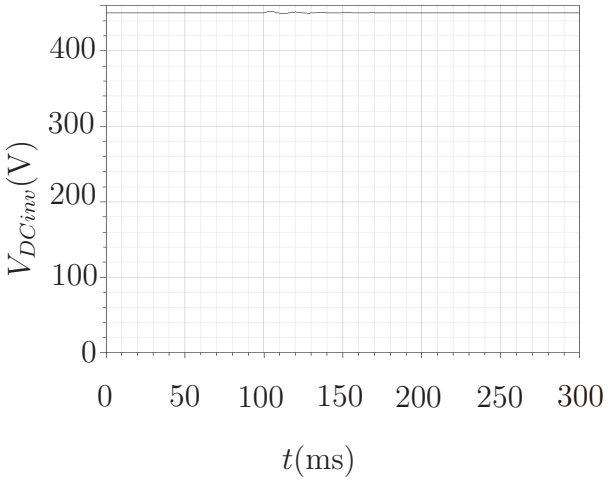

Figure 4.14 – Inverter Control

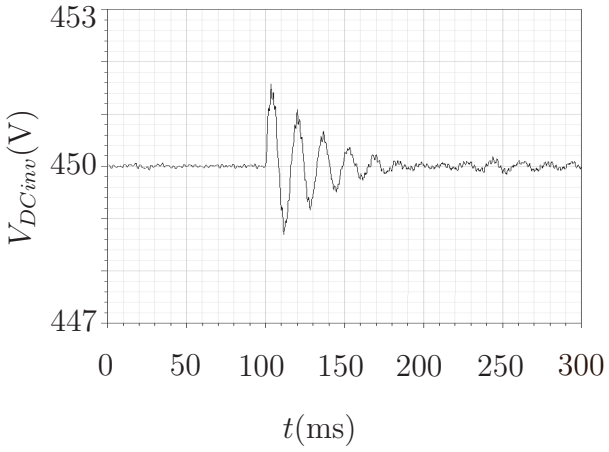

Figure 4.15 – Inverter Control - Enlarged

4.4.2 Practical System Implementation

Both of these controller is implemented on the FPGA controller board. The rectifier- and inverter controllers are tested and measured separately because the supply voltages need to be manually adjusted.

The current controller is tested and measured first. The current I_{line} is measured while a change in the supply voltage V_{ACrec} is made. Figure 4.16 shows how the rectifier controller responds to a change in supply AC voltage (V_{ACrec}). The top trace shows the supply AC voltage V_{ACrec} and the bottom trace shows the line current I_{line}. The change in the supply voltage can be observed at 2000 ms.

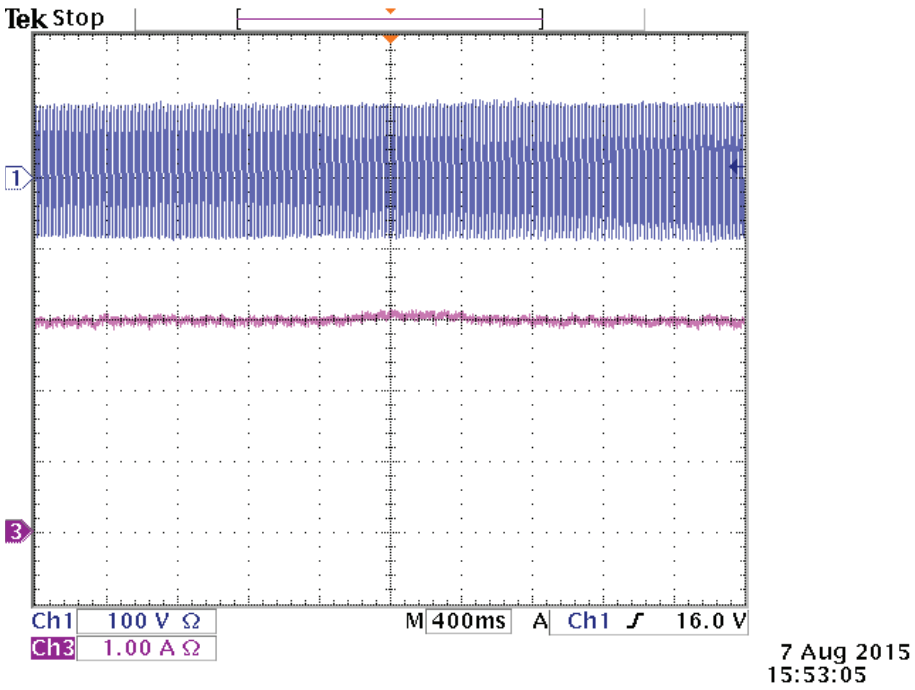

Figure 4.16 – Rectifier Control Results - I_{line}

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The voltage V_{DCinv} is measured while a change in the supply voltage V_{ACinv} is made. Figure 4.17 shows how the inverter controller responds to a change in supply AC voltage (V_{ACinv}). The top trace is the supply AC voltage V_{ACinv} and the bottom trace shows the inverter DC voltage V_{DCinv}. The change in the supply voltage can be observed at 1200 ms.

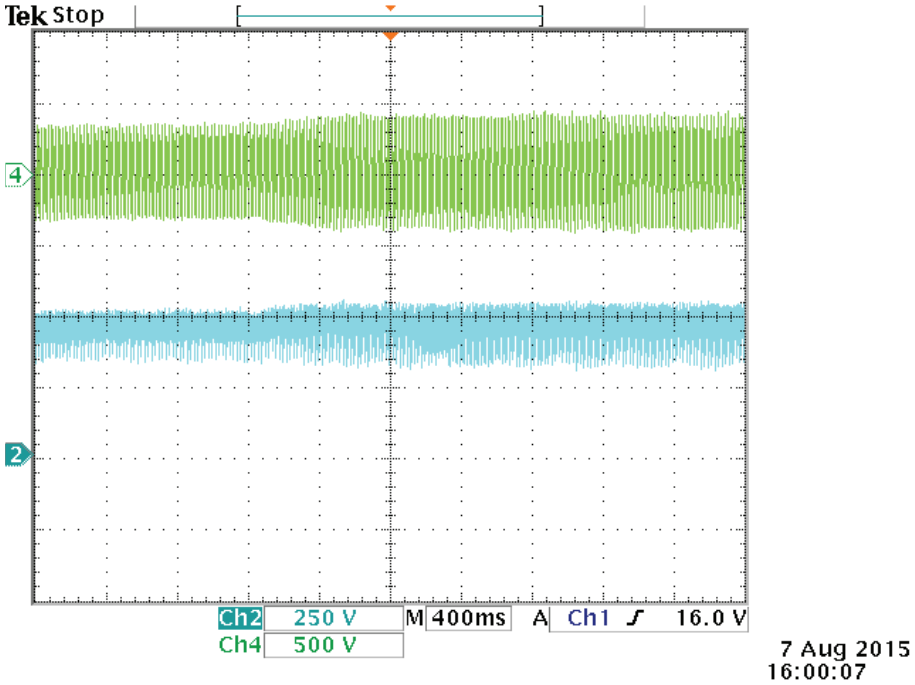

Figure 4.17 – Inverter Control Results - V_{DCinv}

During both tests the controllers continued to regulated the current or voltage successfully after the change in supply voltages. Both of the controllers also reacted within their specifications. Constant power transfer is achieved and therefore the controller implementations are successful.

It is concluded that a practical HVDC Terminals model is constructed with adequate controllers implemented at both thyristor converters. The HVDC Terminals model is suitable to successfully test a HVDC Series Tap model.

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4.5 Summary

In this Chapter the design, simulation and implementation were discussed. First the rectifier transfer function was determined and the rectifier controller designed and simulated. Thereafter, the inverter transfer function was determined subsequently the inverter controller was designed and simulated. Next, a system level simulation was performed. Lastly, both controllers were practically implemented and the practical measurements were presented.

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Chapter 5

HVDC Series Tapping Options

5.1 Introduction

This Chapter discusses several previously proposed series taps. Thereafter, several tapping option were devised and simulated. The results of these simulations are compared in terms of their efficiency, switch utilisation, number of IGBTs required, number of diodes required, reliability and complexity.

5.2 Series Tap Requirements

According to [11], a series tap should have the following characteristics: minimum cost, no reduction of transmission line reliability and the tap control must be independent of the main terminal control.

Series tapping is used to create a more economically viable option in comparison to parallel tapping. A parallel tap of the same power rating would use several high voltage components to achieve the required voltage rating for the parallel tap. Components of a lower rating can be used, therefore creating a less expensive tap [9].

The presence of a series on a tap should not compromise the reliability of the HVDC transmission line it is connected to. HVDC transmission systems typically deliver fairly large portions of power. The loss of such portions of the power system may lead to a system wide collapse.

The controls of the series tap should be self-contained. This eliminates the need for fast inter-terminal communication; as is the case for parallel taps. This reduces the cost of the tap and simplifies its operation. The control of the series tap should not interfere with the controls of the terminal controls of the HVDC transmission system.

The main issue encountered during the conceptualisation of different options is how to provide adequate insulation between the line potential and the earth potential while delivering power.

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An important design choice is the maximum voltage drop across the series tap. If the voltage drop is too high, it could interfere with the control of thyristor bridges on both sides of the HVDC transmission line. Should the voltage drop be too low, the required power rating will not be reached.

Several series tapping topologies creates a DC bus voltage from the line current of the HVDC transmission line by use of a converter. The three phase voltages are created using another converter connected to the local AC network. Figure 5.1 shows where the intermediate bus voltage is situated in such converters.

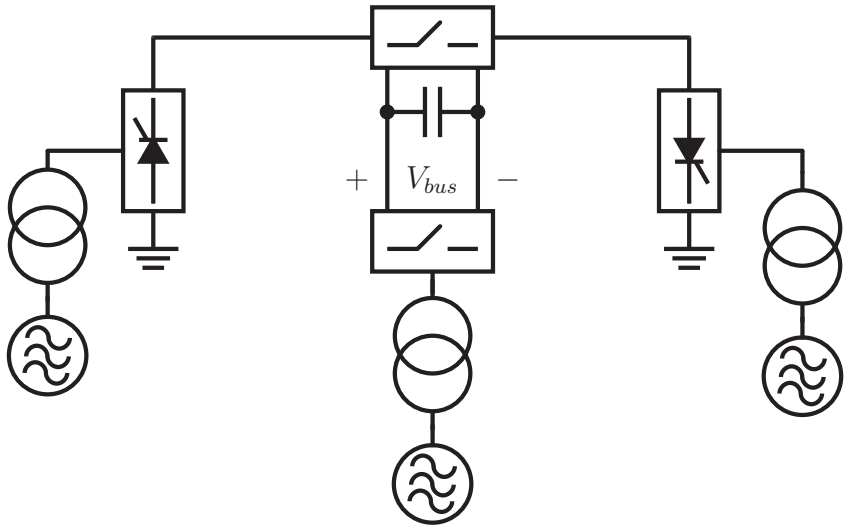

Figure 5.1 – Intermediate DC bus Voltage

Another design choice which has to be made is the DC bus output voltage. This voltage is supported by either a capacitor or batteries. In the case of a large DC bus capacitor, a capacitance of several millifarads is required to filter the voltage ripple. When choosing a bus capacitor, the available voltage ratings of such large capacitors should be considered. The output DC bus voltage was chosen to be 2 kV. The paramount issue that needs to be resolved in any series tap is how to isolate the DC voltage of the HVDC transmission line from the locally connected AC network. Each of the proposed series taps will be compared according to efficiency, switch utilization, the number of IGBTs and diodes required, reliability and complexity [50].

Energy can be transferred in several different ways. Each of these ways present a solution to provide adequate isolation. Electromagnetic, mechanical and electrochemical energy transfer is each investigated as a possible means to provide galvanic isolation.

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5.3 Previously Proposed Taps & Applicable Technologies

In the past, several series tap schemes have been proposed. Some of these are discussed below.

In [9], a series tapping scheme is proposed using a 12-pulse thyristor bridge. A DC machine is connected to the DC line and used to drive an AC generator. In turn, the AC generator provides the voltages required to commutate the thyristor bridge. A power transformer provides isolation between the DC line and the AC network. From the simulation results, it was shown that the proposed scheme is feasible.

A series tap based on forced commutated converter technology is proposed in [12]. As an example, the tap delivers 5 MW from a DC line that operates at 75 kV. The proposed tap was simulated successfully. Due to forced commutation, it was found that the tap was not as sensitive to AC disturbances as a similar parallel tap using line commutated thyristor bridges.

A different forced commutated converter series tap is proposed in [13]. This series tap used three power converter stages to tap power from the DC line and deliver it to a local AC network. Because of the three different stages required for the tap to operate, tap losses slightly increased. Simulations showed that this tap have good dynamic properties.

The use of an air-core transformer to provide galvanic isolation is mentioned in [11]. In [14], [15], and [16], this concept is explored and a topology is proposed. GTOs are suggested as switching devices. A full-bridge of four GTO's are used to send pulses to a transformer. On the secondary side of the transformer, the AC voltage is rectified by means of a diode bridge and a capacitor is used to create a DC bus. From this DC bus, a three phase converter is used to create an AC voltage. A digital simulation was used to confirm the scheme's technical feasibility. According to the results 1 MW of power could be delivered.

A 25 MW soft-switched series tap that is used on a $\pm$500 kV transmission line is proposed in [17]. The scheme consisted of minimal number of components. An air-core transformer was used to provide isolation. The scheme's control functioned independently from the main converter stations. The simulation result shows that the tap functions well and responds well to disturbances.

The use of inductive power transfer technology to build a HVDC series tap is proposed in [51]. Simulations show this topology to be a viable option.

In [52], the concept of using energy storage units to provide galvanic isolation between different inter-connected grids is discussed. The principle is that a storage unit is charge at a first grid, disconnect from that grid and connected to a second grid to be discharged, thereby delivering power to the second grid. The concept of using energy storage in a series tap is proposed in [53]. Energy storage allows the tap to function even if the DC line current is low.

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Some storage units mentioned are sodium-sulphur batteries and super-capacitors, although further research in these areas are still required. According to [54], sodium-sulphur batteries have a charge/discharge cycle that is 90 % efficient, no memory effect, no self-discharge and a lifespan of 4 500 cycles.

Although several feasible series tapping schemes have been proposed and simulated, a standard practical solution to series tapping is yet to be applied in practice.

5.4 Evaluated topologies

Four different topologies are evaluated. Each of these topologies utilises a different approach to provide galvanic isolation between the DC operating line and ground potential. The first and second option uses an air-core transformer to provide galvanic isolation.

A motor and generator is used to provide galvanic isolation in the third option. The fourth option makes use of energy storage units to provide galvanic isolation.

A simulation of each option is performed in Simplorer 12. This is done, firstly, to provide proof that the chosen topology works with the given simulation parameters. Secondly, current and voltage plots of the topology can be observed. Lastly, information that is required for efficiency and switch utilisation calculations are obtained. These calculations will be used when comparing one topology's performance to another.

5.4.1 Option 1

The first series tap option was first discussed in [55] and revised in [17]. The tap delivers power to a DC bus capacitor from the HVDC transmission line through an air-core transformer and a diode rectifier bridge. Figure 5.2 shows the circuit diagram of the topology. The air-core transformer is used to provide galvanic isolation between the line and ground potential. An H-bridge consisting of two IGBTs, two diodes and a snubber capacitor is used as a soft switching device.

A simulation is performed on the topology given in [17]. The duty cycle was adjusted so that the required power was delivered to the load. The simulation parameters used in the simulation is shown in Table 5.1. Figure 5.3 shows the output voltage. Figure 5.4 shows the voltage across the series tap.

5.4.2 Option 2

The second option is another topology that uses an air-core transformer to provide galvanic isolation. A current source to voltage source converter is used to create a bus voltage. The air-core transformer is then resonantly driven with compensating capacitors. The switching

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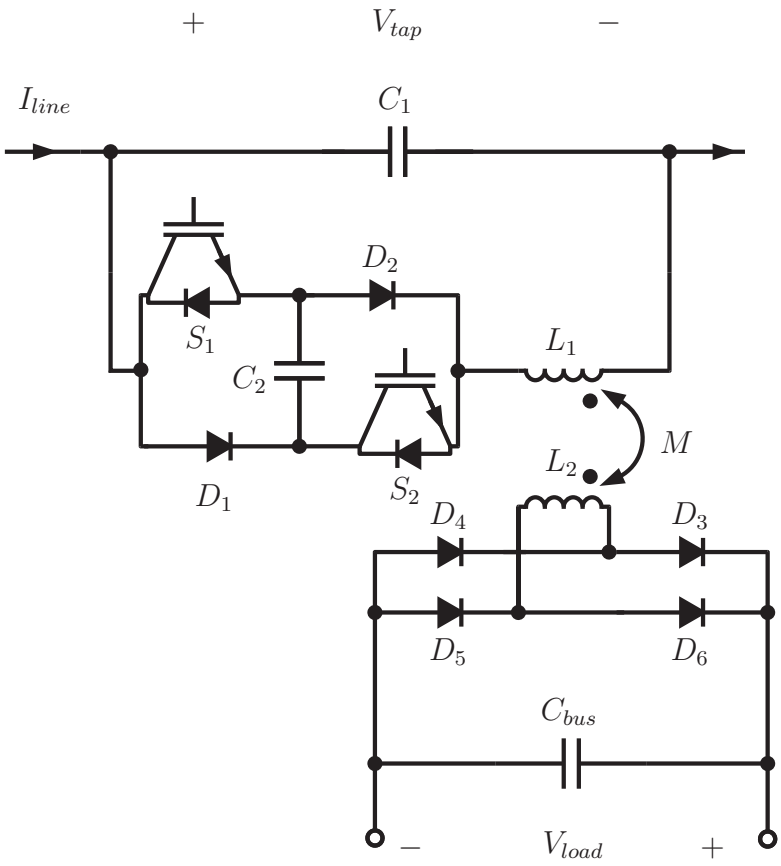

Figure 5.2 – Option 1 Circuit Diagram

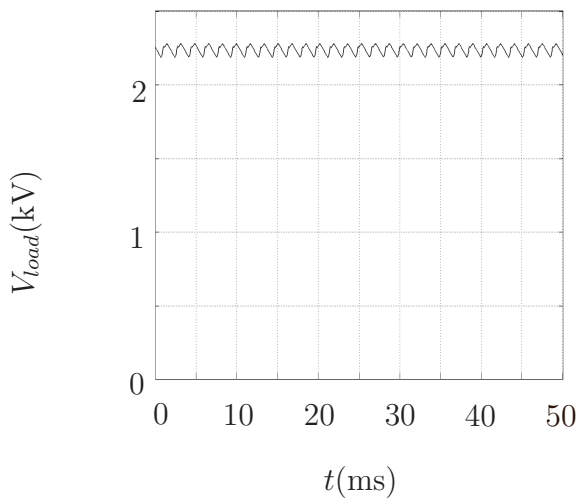

Figure 5.3 – Option 1 Output Voltage

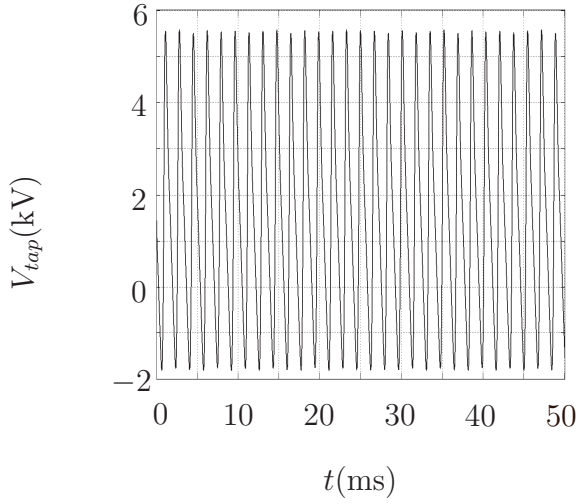

Figure 5.4 – Option 1 Tap Voltage

frequency is chosen at the resonant frequency of the compensated air-core transformer. This topology was first suggested in [50].

A simulation is performed on the topology given in [17]. The duty cycle was adjusted so that the required power was delivered to the load. The simulation parameters used in the simulation is shown in Table 5.2. Figure 5.3 shows the output voltage. Figure 5.7 shows the voltage across the series tap.

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I_L	1800 A
V_O	2.23 kV
C_1	45 μF
C_2	10 μF
L_1	15 mH
L_2	0.6 mH
M	2.25 mH
C_{bus}	10 mF
f_s	587 Hz
D	0.7525

Table 5.1 – Option 1 Simulation Parameters

I_L	1800 A
V_O	2.23 kV
C_1	10 mF
C_{11}	4.26 μF
C_{22}	25.79 μF
L_{11}	15 mH
L_{22}	0.6 mH
M	2.25 mH
L_{filter}	1 mH
C_{filter}	10 μF
f_s	587 Hz
D	0.561

Table 5.2 – Option 2 Simulation Parameters

5.4.3 Option 3

The third option uses mechanical energy transfer to provide galvanic isolation. A motor is driven by a three-phase motor drive that is powered from the HVDC transmission line. The motor is connected to a generator by a shaft that is made of an insulating material. Such materials include carbon-fibre or fibre glass. The length of the shaft must be sufficient to provide galvanic isolation. This topology was first suggested in [50]. Figure 5.8 shows the diagram of the topology. Table 5.3 shows the simulation parameters of the current source to voltage source converter.

C_1	10 μF
f_s	587 Hz
D	0.445

Table 5.3 – Option 3 Simulation Parameters

5.4.4 Option 4

The fourth option uses energy storage units, possibly sodium sulphur batteries or super capacitors, to provide galvanic isolation by the connection and disconnection of these units by the

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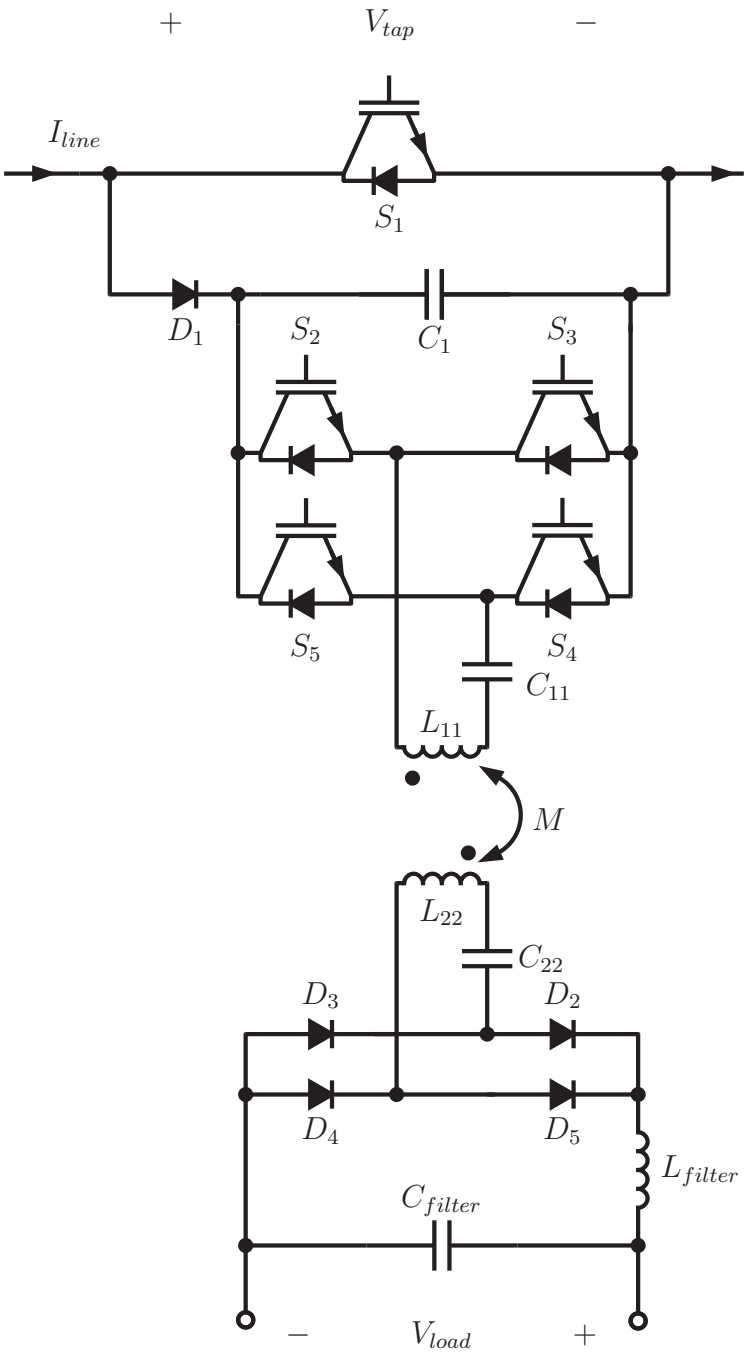

Figure 5.5 – Option 2 Circuit Diagram

open and closing of switches S_3 to S_{14}. Figure 5.9 shows the diagram of the topology. Table 5.4 shows the simulation parameters of the current to voltage source converter.

This topology was first proposed in [50]

C_1	$10\,\mu$F
f_s	587 Hz
D	0.445

Table 5.4 – Option 4 Simulation Parameters

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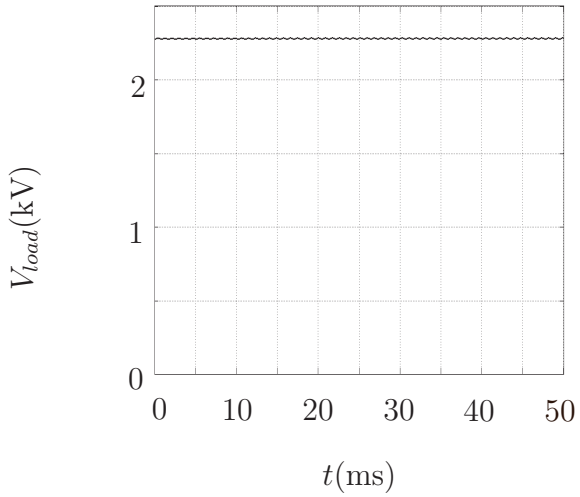

Figure 5.6 – Option 2 Output Voltage

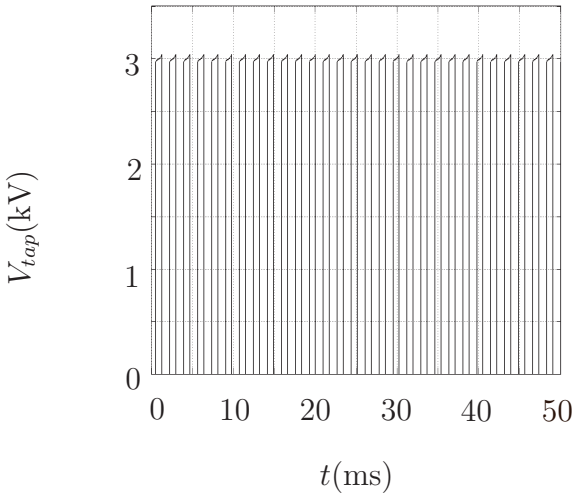

Figure 5.7 – Option 2 Tap Voltage

5.5 Comparison

The different options were compared in terms of efficiency, switch utilisation, number of IGBTs used, number of diodes used and complexity. The results are summarised in Table 5.5.

Switch utilisation is a number between zero and one. It is calculated by dividing the output power of the converter by the product of the peak current and peak voltage the switch has to withstand [24].

During the efficiency calculations several assumptions have been made. The efficiency of each option includes a three-phase inverter connected to the output bus voltage of each option.

The first being that the same IGBTs and diode will be used for each design. The required voltage and current rating will be achieved by series and parallel combinations of IGBTs or diodes and that current will divide equally among parallel switches and that a snubber is present on series connected switches that facilitates equal voltage division. For the calculation of IGBT switching and conduction losses, the properties of the FZ750R65KE3 IGBT from Infineon Technologies [56] is used. The properties of the DRD5150H65 rectifier diode from Dynex Semiconductors [57] was used to calculate the diode losses.

The second being that induction machines and a three-phase generators are 95 % efficient. According to [58], electrical machines are between 85 % and 97 % efficient. The assumption is based on these values.

The third is that air-core transformer losses are dominated by conduction losses. The air-core transformer found in [17] in both option that use an air-core transformer. The resistances of each winding is specified and is used to calculate conduction losses of each winding.

The fourth assumption is that the charge and discharge cycle of an energy storage unit is 90 % efficient.

The last assumption is that a three-phase inverter and other converters are 90 % efficient.

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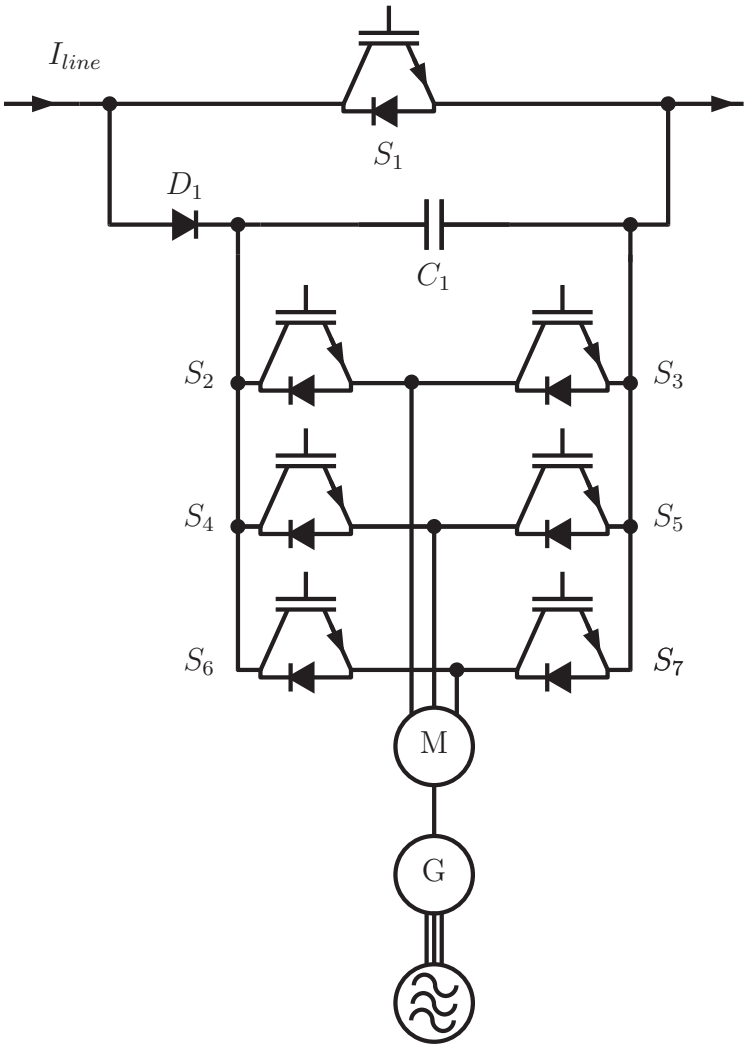

Figure 5.8 – Option 3 Circuit Diagram

The number of IGBTs include the IGBTs required for the three-phase inverter connected at the output bus voltage of each.

The calculation of efficiency and switch utilisation requires the voltage- and current waveforms of each relevant element. The switching losses are calculated by using the switching energy that is specified in the IGBT's datasheet [56]. The average and RMS values of these waveforms are required to calculate conduction losses. The peak voltage and current values are required to calculate the switch utilisation. Each of these values are calculated by the simulation and used in the different calculations.

The efficiency of an option consisting of several stages is calculated as follows. Firstly, the efficiency of each stage is determined by calculation or assumption. Then the overall efficiency is calculated by multiplying the efficiency of each stage with each other.

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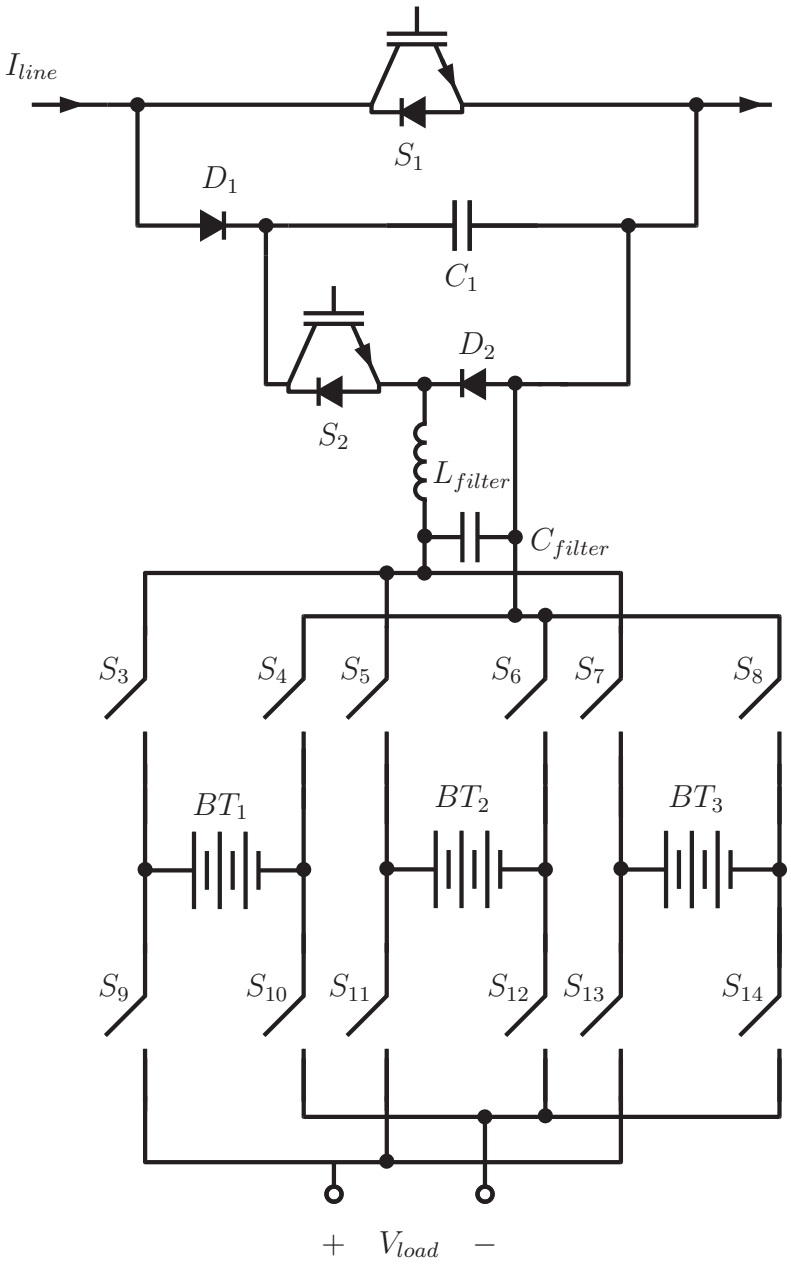

Figure 5.9 – Option 4 Circuit Diagram

5.6 Conclusion

From the results in Table 5.5 show that each option has its own merits.

Option 1 has the advantage of a simple circuit, but requires a large amount of components to achieve the required voltage and current rating. This leads to increased setup cost. The topology also has the least switch utilisation of the four considered topologies.

Option 2 has the highest efficiency of the considered topologies. This topology also have the best switch utilisation for some of its switches.

Option 3 has the ability to connect directly to the local AC network, because a generator is used to generate the three-phase voltages. Additional control for the generator must be included if

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Tap Design	Efficiency	Switch Utilization	IGBTs	Diodes	Complexity
Option 1	68%	S_1 and S_2 0.017	45	13	Low
Option 2	85%	S_1 0.408 S_2 to S_5 0.552	33	5	High
Option 3	80%	S_1 0.547	21	1	Low
Option 4	72%	S_1 0.549	20	2	Low

Table 5.5 – Comparison of Different Tapping Topologies

the generator must synchronise with an existing AC network.

Option 4 has the lowest efficiency of all the topologies considered. This topology has the advantage that energy storage is inherently part of its operation. This would allow the local AC network to function during low or no current conditions on the HVDC transmission line.

Option 1 provides the most simple circuit, but has poor efficiency and switch utilisation. Option 2 proved to be the most efficient and has the best switch utilisation. But both of these topologies use an air-core transformer that leads to a cheaper tap.

Option 3 provides efficiency that compares favourably with that of topology 1 and 2, but has a mechanical part and therefore would need additional maintenance.

Option 4 provides additional benefits, but at an increased additional cost because of the storage units. Because of the increased cost, another topology will be studied.

Option 1 and Option 2 were chosen for further study in subsequent chapters. Option 1 will be discussed in Chapter 7 and Option 2 will be discussed in Chapter 8. Both these designs utilise an air-core transformer to provide the required isolation. The next chapter will discuss the design and simulation of an air-core transformer.

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Chapter 6

Air-core Transformer Analysis & Simulation

6.1 Introduction

In the previous Chapter, two series tapping topologies was chosen for analysis in further chapters. Each of these topologies utilise air-core transformers to provide the required insulation from the line potential to ground potential. The air-core transformer has the advantages that it will be lighter than an iron-core transformer and that the construction of the transformer and the supporting structure will be cheaper.

A procedure to analyse and design an air-core transformer is needed. A procedure is provided in the subsequent sections.

6.2 Theoretical Overview

This section gives an overview of several technical topics required to complete the analysis and numerical computation.

6.2.1 Self Inductance & Mutual Inductance

According to [59], self-inductance is the parameter that relates a time-varying current to a voltage. The voltage across the inductor is given by the inductance times the time derivative of the current, as shown in Equation 6.2.1.

$$v = L\frac{\mathrm{d}i}{\mathrm{d}t} \tag{6.2.1}$$

Inductance is created by the magnetic field coupling with the conductor carrying that same current. Therefore the name self-inductance. Mutual inductance is when the magnetic field

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created by a first conductor couples to a second conductor and the magnetic field of the second conductor couples with the first conductor. The coupling from the first to the second will be equal to the coupling from the second to the first.

Coils are commonly used to make inductors.

Should two coils be placed in close proximity to one another, there will be coupling between the first coil to itself and the second coil. Similarly, the second coil will have magnetic coupling with itself and the first coil. Therefore, should two coils be used to form coupled inductors, the circuit model will always include the two self-inductances of each coil and the mutual inductance between the two coils.

Figure 6.1 shows the circuit diagram circuit used for a mutual inductance transformer.

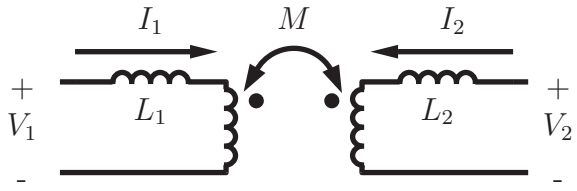

Figure 6.1 – Circuit Diagram Symbol of an Air-core Transformer

From the circuit diagram, it is shown that each winding has its own self-inductance, as well as a mutual inductance. The equations relating the currents and voltages are shown in equations 6.2.2 and 6.2.3.

$$V_1 = L_1 \frac{di_1}{dt} + M \frac{di_2}{dt} \tag{6.2.2}$$

$$V_2 = L_2 \frac{di_2}{dt} + M \frac{di_1}{dt} \tag{6.2.3}$$

Given a specific electromagnetic structure, the self-inductances and the mutual inductance must be calculated. This problem will be analysed in the next section. [60].

The coupling factor is an indication how much of the magnetic field of one coil couples to the other. It is a unitless number between zero and one. Equation 6.2.4 gives the definition of the coupling factor.

$$k = \frac{M}{\sqrt{L_1 L_2}} \tag{6.2.4}$$

6.2.2 Air-core Transformer Model

Power transformers are constructed with an iron lamination core. Because of several limiting factors of conventional power transformers, it was decided that an air-core transformer will be

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investigated as an alternative. The benefits of using an air-core transformer is mentioned in Section 6.1.

Air-core transformers are typically used in high-frequency circuits. The exciting current of a transformer is the current required to induce a voltage at the secondary winding of a transformer. The exciting current of an iron-cored transformer is a small percentage of the load component of the primary current. In the case of an air-core transformer, the exciting current is the entire primary current. The voltage induced at the secondary winding is proportional to the mutual inductance [49].

In [11] the use of an air-core transformer for an HVDC series tap is proposed for the first time. In [14] a method to model an air-core transformer is discussed. The air-core transformer analysed in [14] consisted of two coils placed on top of each other.

Another topology using an air-core transformer is proposed in [17]. The air-core transformer consisted of two coils placed within one another.

The advantage of placing the primary coil within the secondary coil is that a greater portion of the magnetic flux intercepts the secondary coil. Therefore, better coupling is achieved. The air-core transformer is analysed in this section is of similar construction.

6.2.3 Pashen's Law

Air will mainly be used as an insulating medium in the air-core transformer. The electrical strength of air needs to be calculated so that there is sufficient clearance between the primary and the secondary winding, and between the turns of each coil to allow reliable operation of the air-core transformer.

Paschen's Law related the breakdown voltage of a uniform electric field between two electrodes. For the purpose of the simulation, the electrodes will be the turns of the air-core transformer. It is also assumed that the electrical field between the turns are uniform. Paschen's Law was studied in [61], [62] and [63]. The breakdown voltage (V_B) for air at 20 °C is given by Equation 6.2.5, with p defined as the air pressure, d as the distance between the electrodes and a and b as constants.

$$V_B = \frac{apd}{\ln(pd) + d} \tag{6.2.5}$$

with

$$a = 4.36 \times 10^7 \text{ V/(bar.m)}$$
$$b = 12.8$$

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This formula gives the breakdown voltage for a one meter gap in air at 20 °C as $V_B = 2.5\,\text{MV}$. Equivalently it could be said that air has a breakdown strength of 25 kV/cm.

6.3 Physical Description

In this section, the chosen construction of the air-core transformer will be discussed. A mathematical analyses of the air-core transformer follows.

It is decided that the air-core transformer will have two concentric coils. The inner coil will be the primary winding and the outer coil will be the secondary winding. Figure 6.2 shows a top view of the two coils. The radius of the primary winding is defined as r_{pri} and the radius of the secondary winding defined as r_{sec}. The distance between the two coils will determined the breakdown voltage. The difference is defined as follows: $r' = r_{sec} - r_{pri}$. Each winding will consist of several turns.

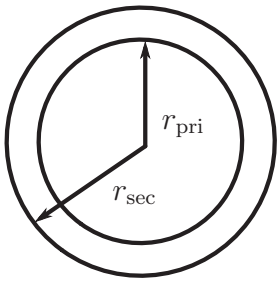

Figure 6.2 – Air-core Transformer Inter-coil Definition

Each coil is defined in terms of their pitch and their height. Figure 6.3 shows how each winding is defined in terms of their pitches (p_{pri} and p_{sec}) and their height (h_{pri} & h_{sec}).

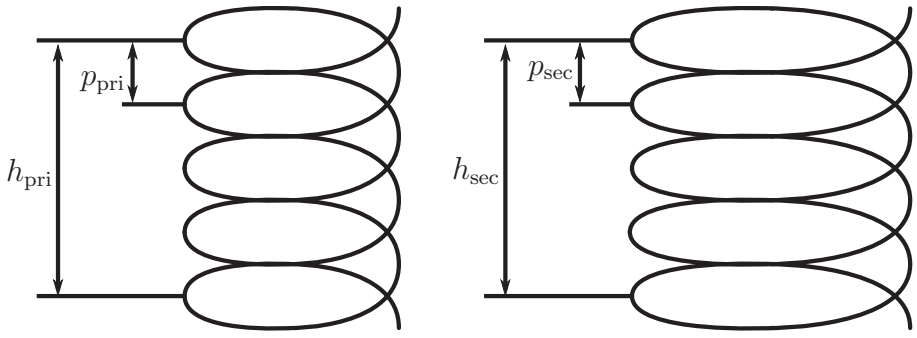

Figure 6.3 – Air-core Transformer Coil Definition

We assume that the voltage across the inductor will divide equally among the turns of the winding. Therefore, the pitch of each turn will determine the breakdown voltage between the turns.

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6.4 Mathematical Description

The object of the simulation is to calculate the self-inductances of the primary and secondary winding and the mutual inductance between the two windings. A mathematical procedure needs to be followed in order to achieve this.

The procedure for calculation the inductance of the primary winding will be discussed. The same procedure will be applied to calculate the self-inductance of the secondary winding and the mutual inductance between them. All equations and definitions is obtained from [64].

The inductance (L) of an electromagnetic structure is equal to the total flux (Φ) enclosed by the structure divided by the current (I) flowing in the conductor causing the magnetic flux, as stated in Equation 6.4.1.

$$L = \frac{\Phi}{I} \tag{6.4.1}$$

In the case of the self-inductance of the primary winding, the electromagnetic structure and the current-carrying conductor is both the primary winding. To calculate the self-inductance of the secondary winding, the electromagnetic structure and the current-carrying conductor is both the secondary winding. However, in the case of the mutual inductance, the electromagnetic structure is the one winding and the current-carrying conductor is the other winding. It does not matter which winding performs which role, the mutual inductance will be the same.

Subscripts are used to denote which entity relates to which winding. The subscript of entities relating to the primary winding will have a subscript of 1. Likewise entities relating to the secondary winding will have a subscript of 2. For inductance, it is of importance to know which winding is enclosing magnetic flux and which winding is the carrying conductor. The first number of the subscript will indicate which winding is carrying the current and the second number will indicate which winding is enclosing the magnetic flux. For magnetic flux, it is important to know which winding is creating the magnetic flux density and across which winding's surface is being integrated. The first number of the subscript indicates which winding creates the magnetic flux density and the second number of the subscript indicates across which winding's surface is being integrated.

The self-inductance of the first winding is being calculated; therefore both numbers are the same. The subscript of the inductance being calculated and the magnetic flux being used for the calculation must be the same, otherwise the wrong entity is associated with the calculation.

The magnetic flux (Φ) encloses by the structure is equal to the integral across the enclosed surface of the dot product of the magnetic flux density ($\bar{B}$) created by the current flowing in the conductor (I) and the differential surface ($\mathrm{d}\bar{s}$) of the structure, as shown in Equation 6.4.2.

$$\Phi_{11} = \int_s \bar{B}_1 \cdot \mathrm{d}\bar{s}_1 \tag{6.4.2}$$

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By substituting Equation 6.4.2 into Equation 6.4.1, the following result is obtained:

$$L_{11} = \frac{1}{I_1} \int_s \bar{B}_1 \cdot \mathrm{d}\bar{s}_1 \tag{6.4.3}$$

Next, the magnetic flux density ($\bar{B}$) must be calculated by the use of the Biot-Savart law. The Biot-Savart law calculates the magnetic flux density at a point in space, referred to as the field point, from a current-carrying conductor. The point on the differential length of current-carrying conductor is referred to as the source point. The vector $\bar{R}$ is defined from the source point to the field point.

The Biot-Savart law states that the magnetic flux density at a point is equal to the permeability of free space divided by 4π times the integral along the curve of the current-carrying conductor of the quotient of the cross product of the vector of the current and the vector relating the field point to the source point, and the length of the vector cubed. This is shown in Equation 6.4.4.

$$\bar{B} = \frac{\mu_0}{4\pi} \int_c \frac{I\,\mathrm{d}\bar{l} \times \bar{R}}{|R|^3} \tag{6.4.4}$$

By substituting Equation 6.4.4 into 6.4.3, the following result is obtained:

$$\begin{aligned} L_{11} &= \frac{1}{I_1} \int_s \left(\frac{\mu_0}{4\pi} \int_c \frac{I_1\,\mathrm{d}\bar{l}_1 \times \bar{R}}{|R|^3} \right) \cdot \mathrm{d}\bar{s}_1 \\ &= \frac{\mu_0}{4\pi} \int_s \left(\int_c \frac{\mathrm{d}\bar{l}_1 \times \bar{R}}{|R|^3} \right) \cdot \mathrm{d}\bar{s}_1 \end{aligned} \tag{6.4.5}$$

Similarly, the self-inductance of coil 2 (L_{22}) and the mutual inductance (M) among these coils can be calculated. It is important to note that the mutual inductance remains the same regardless if coil 1 or coil 2 is used as the current-carrying conductor or the enclosing structure. Therefore $M = L_{12} = L_{21}$.

$$\begin{aligned} L_{22} &= \frac{\mu_0}{4\pi} \int_s \left(\int_c \frac{\mathrm{d}\bar{l}_2 \times \bar{R}}{|R|^3} \right) \cdot \mathrm{d}\bar{s}_2 \\ M &= \frac{\mu_0}{4\pi} \int_s \left(\int_c \frac{\mathrm{d}\bar{l}_1 \times \bar{R}}{|R|^3} \right) \cdot \mathrm{d}\bar{s}_2 \end{aligned}$$

6.5 Numerical Analysis

6.5.1 Overview of the simulation

In the previous section it was decided that a numerical solution will be used to calculate the parameters of an air-core transformer. Several assumptions and simplifications are used to complete the simulation. This section discusses the procedure followed during the simulation.

Figure 6.4 shows the process that the simulation follows.

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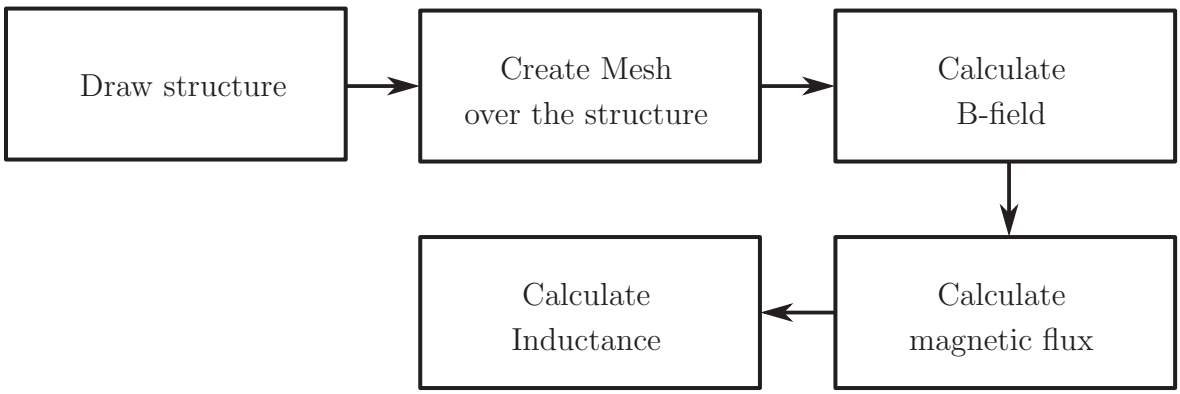

Figure 6.4 – Air-core Transformer Simulation Diagram

The first step is to draw the two windings that will be simulated. This achieved by creating a list of points that describes the structure.

The next step is to mesh the structure so that differential elements are created. Each differential element's influence on a specific entity is then calculated and the effect of each element is the summed together to calculate the overall effect.

The third step is to calculate the B-field, or magnetic flux density, generated by the structure. The magnetic flux enclosed by each winding is then calculated.

The last step is to calculate the self-inductances of each winding and the mutual inductance among then. From these values the coupling factor will be derived.

6.5.2 Simulation process and assumptions explained

It is assumed that the conductor is of infinitesimal width. This is a reasonable assumption given that the radius of the coil is much greater than the width of the conductor.

The shape of the coil will be approximated by representing each turn of the winding as a circle. Figure 6.5 shows how each turn of the winding can be adapted as circles.

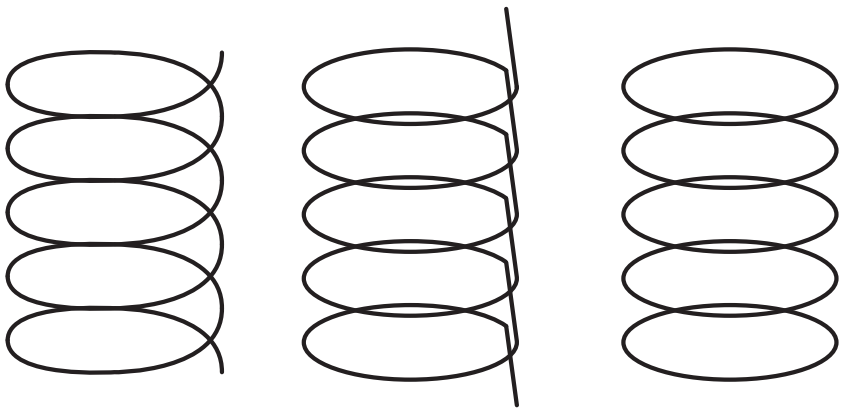

Figure 6.5 – Air-core Transformer Discs

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The winding on the left of Figure 6.5 shows the actual turns of the winding. The middle winding shows how the winding can be alternatively wound so that each turn resembles a circle. For the purpose of the simulation, it is assumed that the conductor connecting the different circles has a negligible effect on the inductance. Therefore it will be ignored to simplify the simulation. The winding on the right of Figure 6.5 shows the structure that will be used during the simulation.

To create the mesh, the number of elements on the diameter of each circle is chosen. Square differential elements are used for simplicity. The centre points of the differential elements are specified. The simulation only uses an odd amount of points, assuring that a point is always on the centre of the circle. The size of the differential element is determined according to the size of the specific circle. Figure 6.6 shows an example of a single circuit with its mesh. The mesh has been chosen to have nine elements across the diameter.

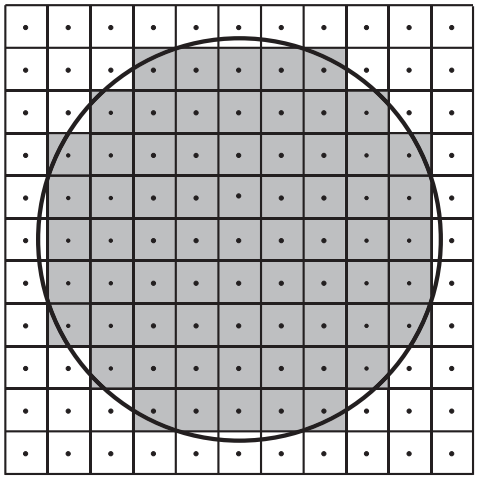

Figure 6.6 – Air-core Mesh

It is important to note that pieces of the area of the differential elements overlap the circle and should not form part of the calculation. Likewise, some enclosed area is not included in the calculation. It is assumed that the area should not be included and the area that is not included is approximately the same, therefore this effect is negligible. The more differential elements is chosen across the diameter, the more accurate the calculation will be.

Each circle will be approximated using polygons. The number of sides of these polygons are specified in the simulation. The straight line pieces of the polygon simplifies the calculation of the magnetic flux density. The magnetic flux density will be calculated for the centre point of each differential element. The polygons are determined by connecting point on the circle.

Should the centre point of the differential element be on the circle, an infinite inductance will be calculated. To avoid such a calculation error, a critical radius is determined. The distance of a point to the centre of the specific circle is then calculated. The point will be included in the calculation only if this distance is smaller than the critical radius. The middle points of the

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sides of the polygon is used to determined the critical radius. Figure 6.7 shows how the critical radius is determined.

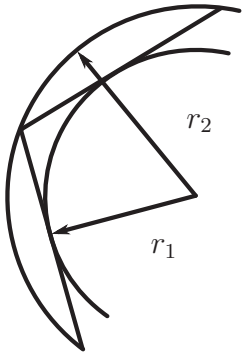

Figure 6.7 – Air-core Circle Approximation

The radius r_2 is the radius of the circle specified in the simulation. The polygon approximation of this circle is shown. The radius r_1 is the critical radius that connects the middle points of the polygon. The more sides the polygon has, the lesser the difference between r_1 and r_2 will be.

6.6 Results

The results of the simulation also converges towards a more accurate value as the number of sides of the polygon approximation is increased and the number of differential elements are increased.

When designing an air-core transformer, the main objective is to achieve the highest coupling factor given the physical constraints of the given design.

The simulation is used to investigate two methods of achieving a higher coupling ratio. The first method investigates the change in coupling factor as the radii of the windings of a single turn air-core transformer is increased. The second method investigates the change in coupling factor as the the number of turns are increased, but the radii of the windings remain constant.

For the first method, the primary- and secondary winding consists each of a single turn. The radius of the primary winding is increased from 1 m to 10 m. The radius of the secondary winding is always 1 m more than that of the primary winding. Figure 6.8 shows how the coupling factor increases with the increase of the radii of the windings.

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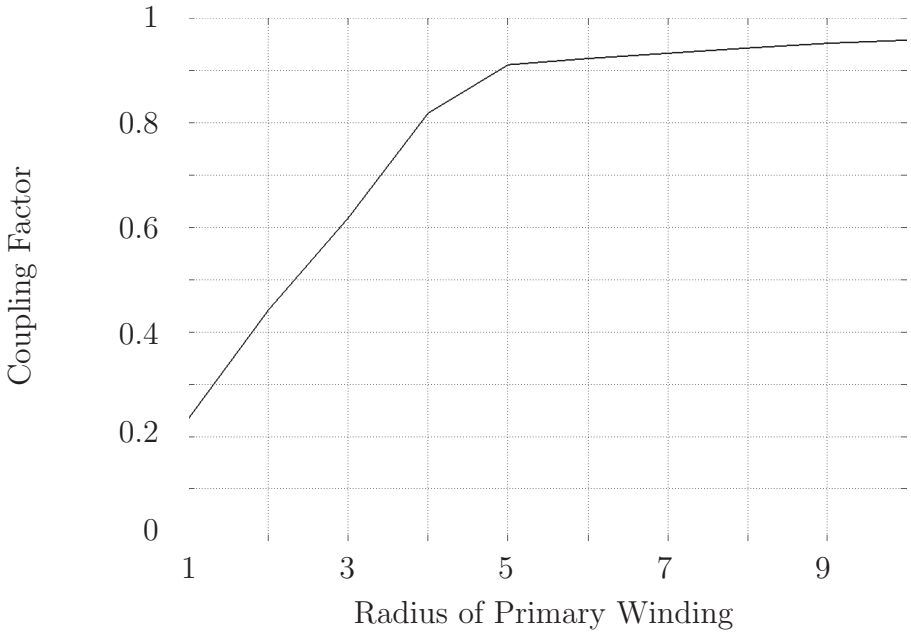

Figure 6.8 – Increasing Radii

The curve is not smooth because of the limited accuracy of the simulation and the radius of the primary winding is also increased in 1 m increments. From Figure 6.8, it is observed that the coupling factor rapidly increases when the radius of the primary winding increases from 1 m to 5 m. The coupling factor has a knee point at 5 m and increases at a lower rate.

For the second method, the radii of the primary winding and the secondary winding are kept constant, but the number of turns are increased. The number of turns of the primary and secondary windings are kept equal. Figure 6.9 shows how the coupling factor increases with the increase of the number of the turns. The top curve is for an air-core transformer with the radius of the primary winding 3 m and the radius of the secondary winding 4 m. The bottom curve shows the coupling factor for an air-core transformer with the radius of the primary winding 2 m and the radius of the secondary winding 3 m.

From Figure 6.9, a knee point is observed on both the top and bottom curves at 3 turns. After 3 turns, the increase in coupling factor is significantly less.

6.7 Conclusion

From the two method that is investigated, it is concluded that the coupling factor can be increased by either increasing the radii of the windings or increasing the number of turns.

The rate at which better coupling is achieved is higher for the first method than the second. Therefore it is suggested that the radii be made as large as possible before more turns are added. It is concluded that the radius of the secondary can be at most 1.2 times the radius of the primary. This ratio occurs at the knee point observed in Figure 6.8.

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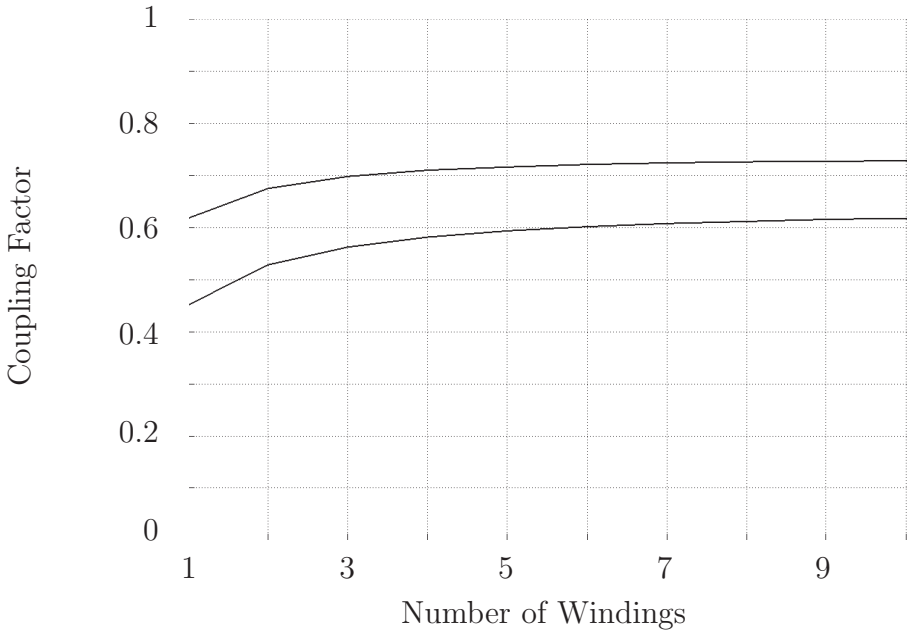

Figure 6.9 – Increasing Windings

From Figure 6.9, it is concluded that the primary and secondary windings should at least consist of three windings.

Although the coupling factor increases more using the first method than the second, it is suggested that a combination of the two methods be used to achieve an optimal solution. Such a solution would provide the most coupling factor for the shortest length of conductor used to construct the air-core transformer.

6.8 Summary

In this chapter the simulation used to calculate the self inductances, mutual inductance and coupling factor were discussed. A theoretical overview was first provided to serve as a basis for the rest of the chapter. The physical description of the air-core transformer was then described. Thereafter, the mathematical description of the simulation was discussed. Subsequently, the numerical method used to calculate the self inductances, mutual inductance and coupling factor was discussed. This section also described the assumptions and approximations used during the analysis. The results were then presented. The chapter ended with a conclusion.

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Chapter 7

First Series Tapping Option Analysis

7.1 Introduction

In this chapter, the first of the chosen topologies will be discussed. This topology was proposed in [17]. The operation of the tap will foremost be discussed. This will be followed by a simulation. Thereafter the differential equations for each state of the converter will be derived. Finally, a conclusion regarding the tap will be presented.

7.2 Operation

Figure 7.1 shows the circuit diagram of the topology. The topology uses two switches (S_1 and S_2), two diodes (D_1 and D_2) and a capacitor (C_2) configured in a H-bridge to achieve soft-switching. This H-bridge functions as a single switch. The capacitor C_1 charges when the line current (I_{line}) flows through it. Once the H-bridge is switched on, the voltage over C_1 appears across the primary winding of the air-core transformer, capacitor C_1 starts to discharge and current starts to flow through the primary winding. A voltage is then induced on the secondary winding of the air-core transformer. This induced voltage is then rectified by the diode bridge (D_3 to D_6) and filtered using capacitor C_3. The capacitance of capacitor C_3 is chosen high enough so that the capacitor can also be used as a bus cap.

Figure 7.2 illustrates how the H-bridge achieves soft-switching and shows the four different states of the cycle that the H-bridge follows. The total current flowing into the H-bridge is referred to as I_{bridge}. The components carrying the current during that state is marked in black. The components that does not carry any current during the same state is marked in grey.

The cycle starts with the top-left state. The states follow one another in a clockwise manner, as indicated by the arrows. The top-left state starts when switches S_1 and S_2 are switched on.

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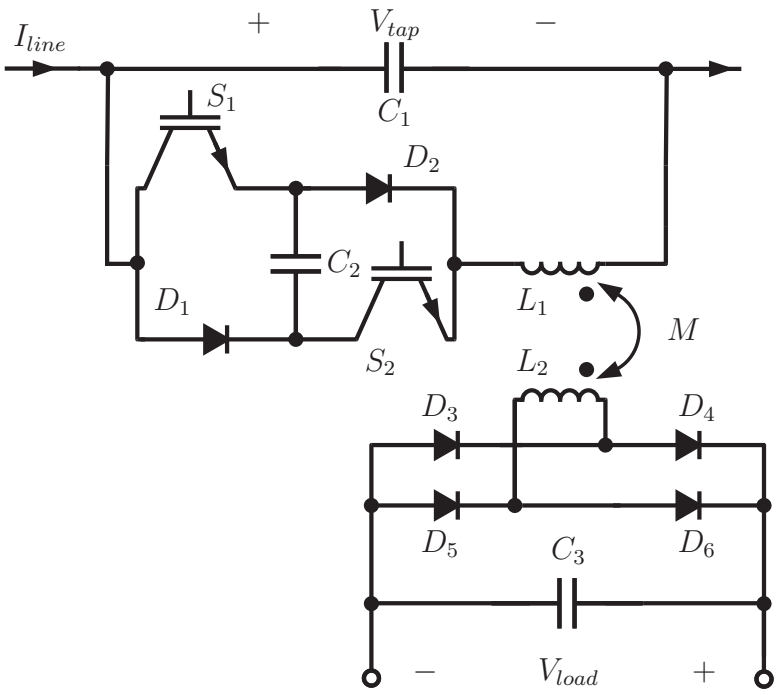

Figure 7.1 – Circuit diagram of Proposed Topology

Capacitor C_2 is already charged. Once the switches are switched on, the current flows through switch S_1 into the negative side on the capacitor and through S_2. The H-bridge goes into the next state once the capacitor is completely discharged.

During this state, the current ceases to flow through capacitor C_2. The two diodes (D_1 and D_2) become forward biased and they start to conduct. At this stage, the current through the H-bridge is shared between the two legs of the H-bridge, the leg consisting of S_1 and D_1 and the other leg consisting of D_2 and S_2. The next state starts once the switches S_1 and S_2 are switched off.

The current now flows through diode D_2 into the positive side of capacitor C_2 and through diode D_1. During this state, capacitor C_2 charges up again. The next state starts when capacitor C_2 is charged again and diodes D_1 and D_2 becomes reversed biased and stop to conduct. This state is the blocking state of the H-bridge. The cycle commences again when the switches S_1 and S_2 are switched on again.

A waveform of the H-bridge operation will be simulated in the next Section.

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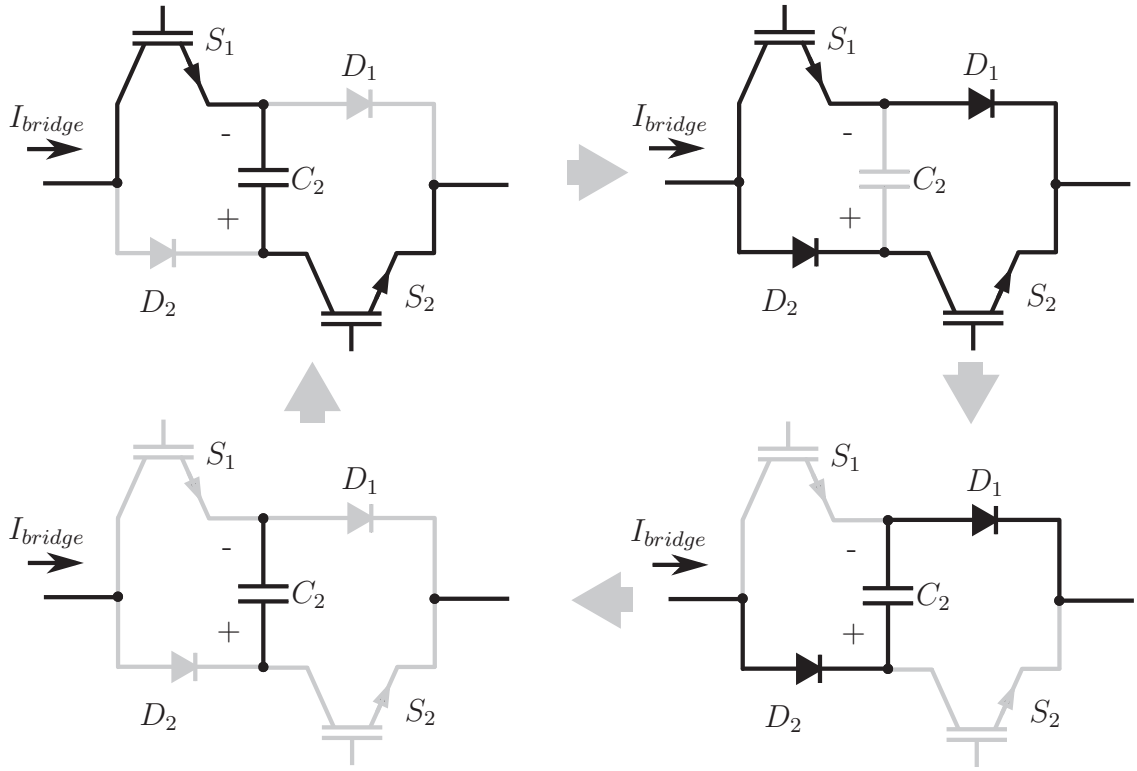

Figure 7.2 – H-bridge Operation

7.3 Simulation

A simulation is performed to confirm the functionality of the topology. Figure 7.3 shows a screenshot of the workspace in Simplorer 15. The same simulation parameters as in Section 5.4.1 of Chapter 5 is used during the simulation.

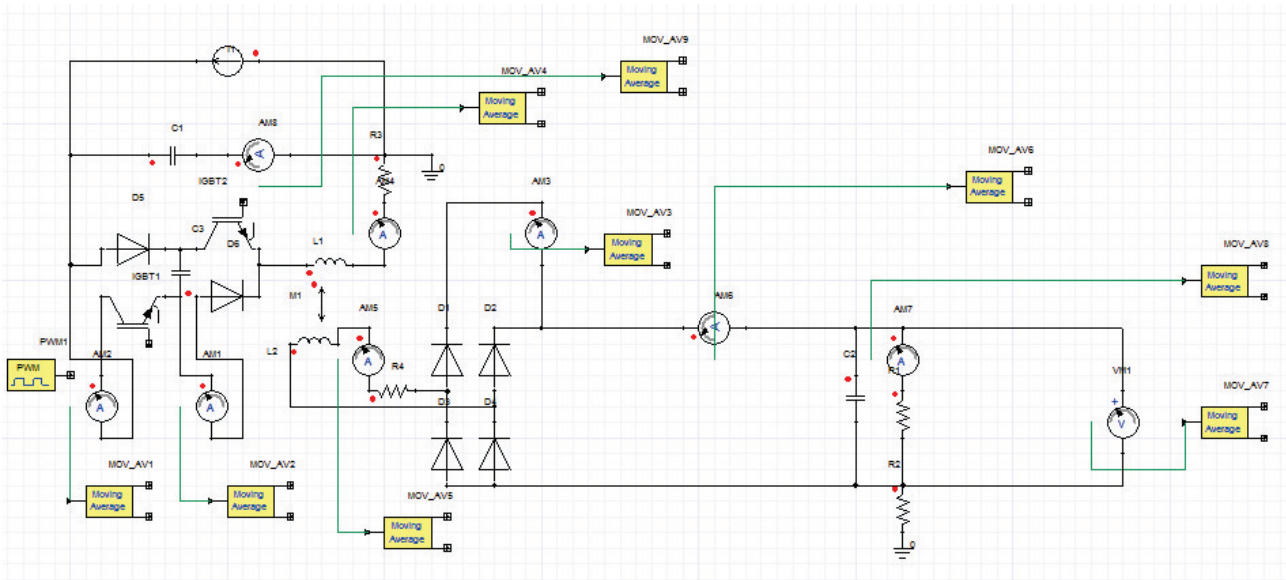

Figure 7.3 – Simplorer 15 Workspace Screenshot

Table 7.1 contains the simulation parameters for the simulation performed.

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Figure 7.4 shows the waveform of the H-bridge operation, as explained in the previous Section and illustrated in Figure 7.2.

Figures 7.7 and 7.8 show the load voltage V_{load} and Figures 7.9 and 7.10 show the load current I_{load} and . The grey trace in both Figures indicate the instantaneous value, whereas the black trace indicates the mean value. It is observed that the load current has a mean value of 1 040 A and ripple of 80 A. Further it is observed that the load voltage has a mean value of 2.1 kV and a ripple of 100 V.

The transformer voltages are shown in Figure 7.5 and the transformer voltages is shown in Figure 7.6. The switches must have adequate ratings to be to handle these currents and voltages.

T_{end}	120 ms
Timestep (min)	1 μs
Timestep (max)	10 μs
I_L	1800 A
V_O	2.23 kV
C_1	45 μF
C_2	10 μF
L_1	15 mH
L_2	0.6 mH
M	2.25 mH
C_{bus}	10 mF
f_s	587 Hz
D	0.7525

Table 7.1 – Simulation Parameters

The total power delivered to the load is calculated by the mean values of the product of load current (I_{load}) and the load voltage (V_{load}). The result is calculated to be 2.18 MW and fulfils the specification that at least 2 MW must be delivered.

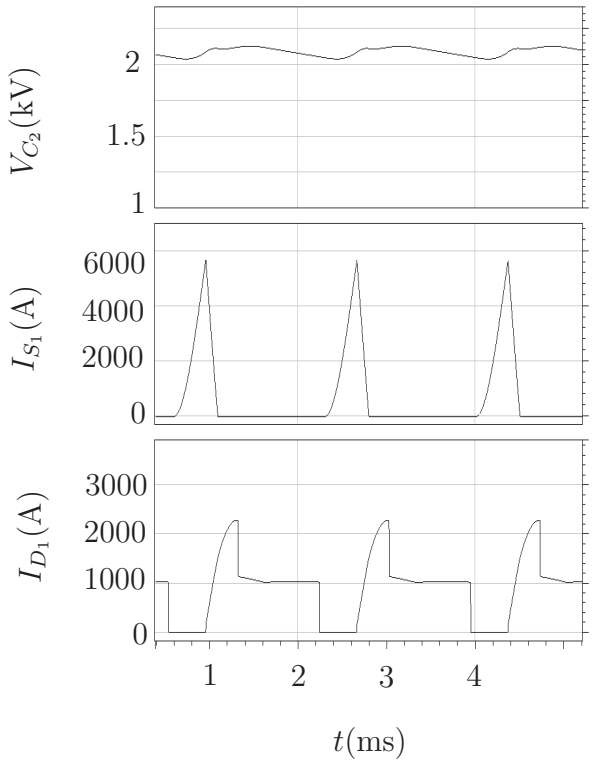

Figure 7.4 – H-bridge Waveforms

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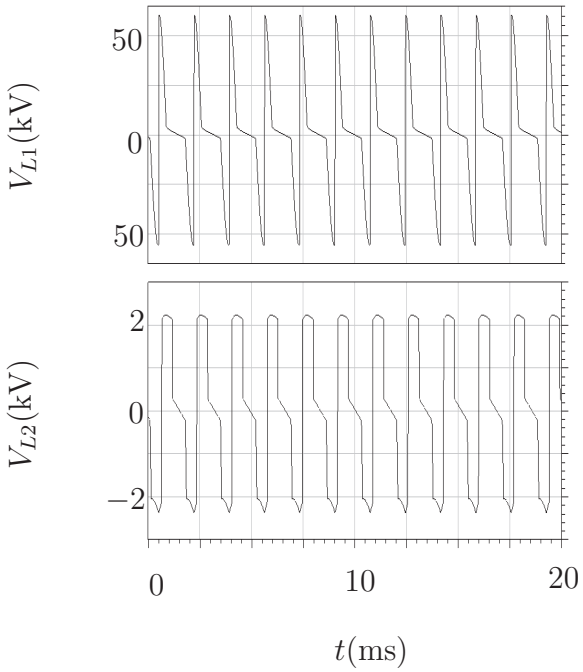

Figure 7.5 – Transformer Voltages - V_{L1} & V_{L2}

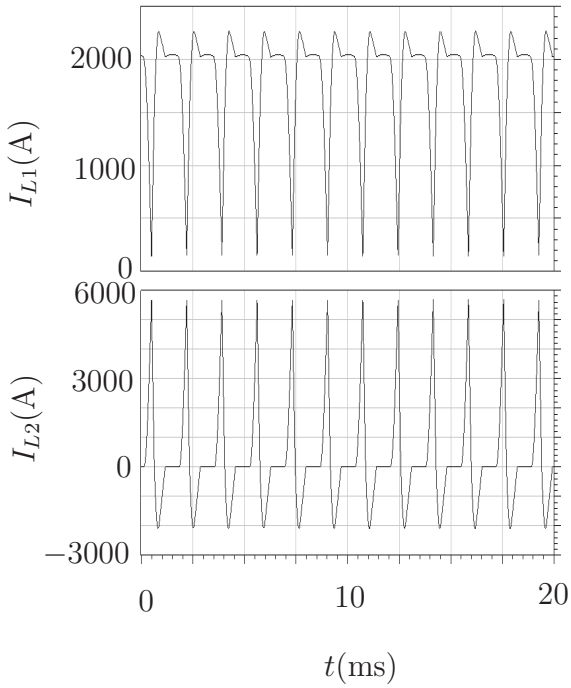

Figure 7.6 – Transformer Currents - I_{L1} & I_{L2}

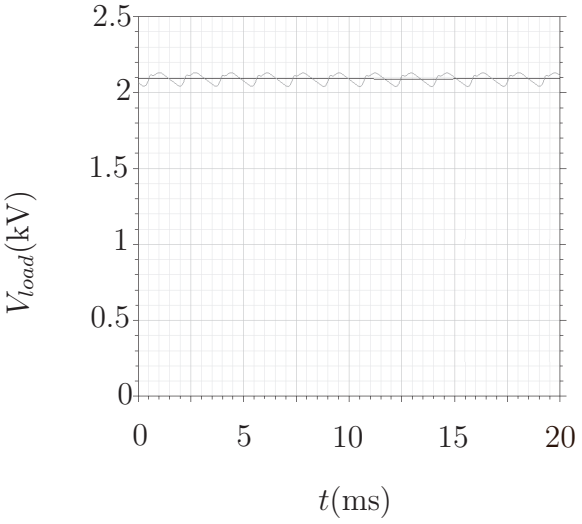

Figure 7.7 – Load Voltage

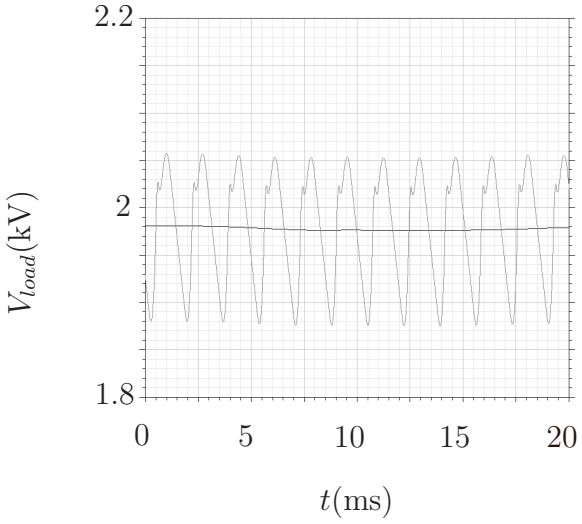

Figure 7.8 – Load Voltage - Enlarged

7.4 Conclusion

Using the simulation performed in Section 7.3, the equivalent circuits of each state and the differential equations of each state, the following conclusion are made:

In a LC series circuit, resonance occurs between these components. Because of resonance taking place between these components, any switches or diodes connected between these components

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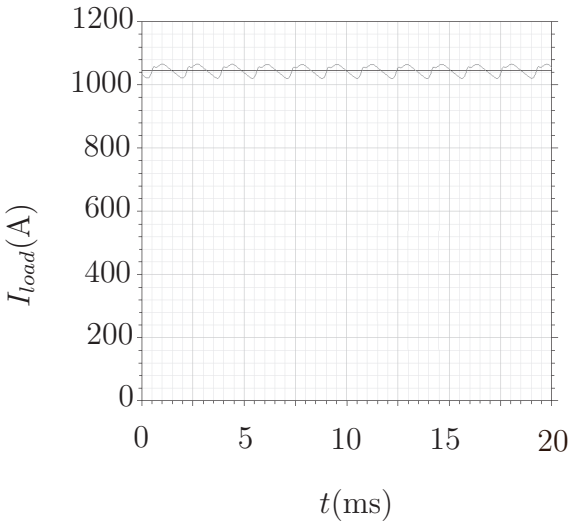

Figure 7.9 – Load Current

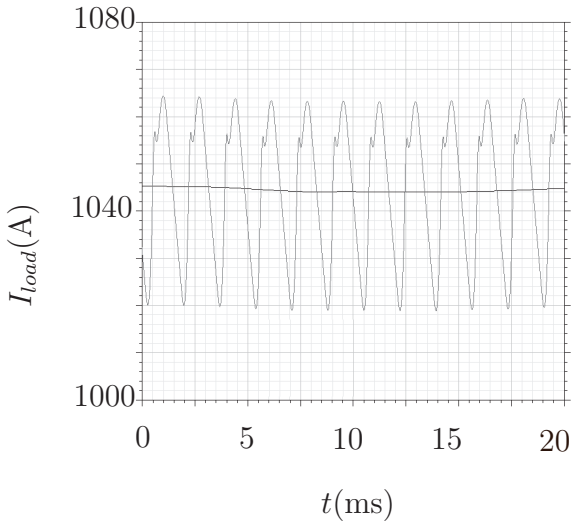

Figure 7.10 – Load Current - Enlarged

will have to be of substantial voltage and current rating to be able to operate at this place in the circuit. Because the ratings required by these switches and diodes and the relative little power delivered in comparison to these ratings, the switch utilisation is very poor. The maximum voltage experienced by the switches S_1 and S_2 and diodes D_1 and D_2 is 57.89 kV and the maximum current is 2263.86 A. The rectifier diodes D_4 D_5 experiences a maximum voltage of 2.13 V and a maximum current of 5663.33 A during the positive half-cycle. During the negative half-cycle, The rectifier diodes D_3 and D_3 experiences a maximum voltage of 2.13 V and a maximum current of 2084.83 A.

Poor switch utilisation implies that a high setup cost will be required where a topology of similar power ratings will cost less to construct. It is therefore concluded that this topology not used to construct the HVDC Series Tap model.

7.5 Summary

In this chapter, the first of the chosen topologies was discussed. The operation of the tap was initially discussed and was followed by a simulation. It was concluded that the switch utilisation of the topology is very low and will therefore have a very high cost in comparison to other topologies of the same rating.

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Chapter 8

Second Series Tapping Option Analysis

8.1 Introduction

A new topology to tap is proposed in [50] and was initially simulated in Section 5.4.2. The simulation in Chapter 5 confirmed that the concept works.

This chapter focusses on a detailed analysis of this series tapping topology. The topology is analysed by deriving the design equations of each stage of the topology.

Thereafter a 2 MW series tap will be simulated using the previous analysis. The design is simulated and the results are discussed.

8.2 Converter Analysis

The topology is analysed in detail in the following section. The topology consists of three stages. Figure 8.1 shows the circuit diagram of the topology with the different stages indicated. Each stage is indicated by a dashed line. The purpose of each stage is shown in the block diagram in Figure 8.2. The purpose of each of these stages are described subsequently.

The first stage of the tap is a current source to voltage source converter. The HVDC transmission line can be modelled as a current source because of the large inductance of the line. The converter charges a capacitor to a specific voltage. The voltage is a function of the duty cycle of the converter. The output voltage of this converter is controlled by varying the duty cycle. Therefore, the output voltage of the converter forms a voltage source. This voltage source, labelled as V_{bus}, feeds the next stage of the converter.

The second stage is the isolation stage. The purpose of this stage is to provide galvanic isolation between the HVDC transmission line and the local AC network. The output of the previous stage is used to drive an air-core transformer. The inductances of the air-core transformer is

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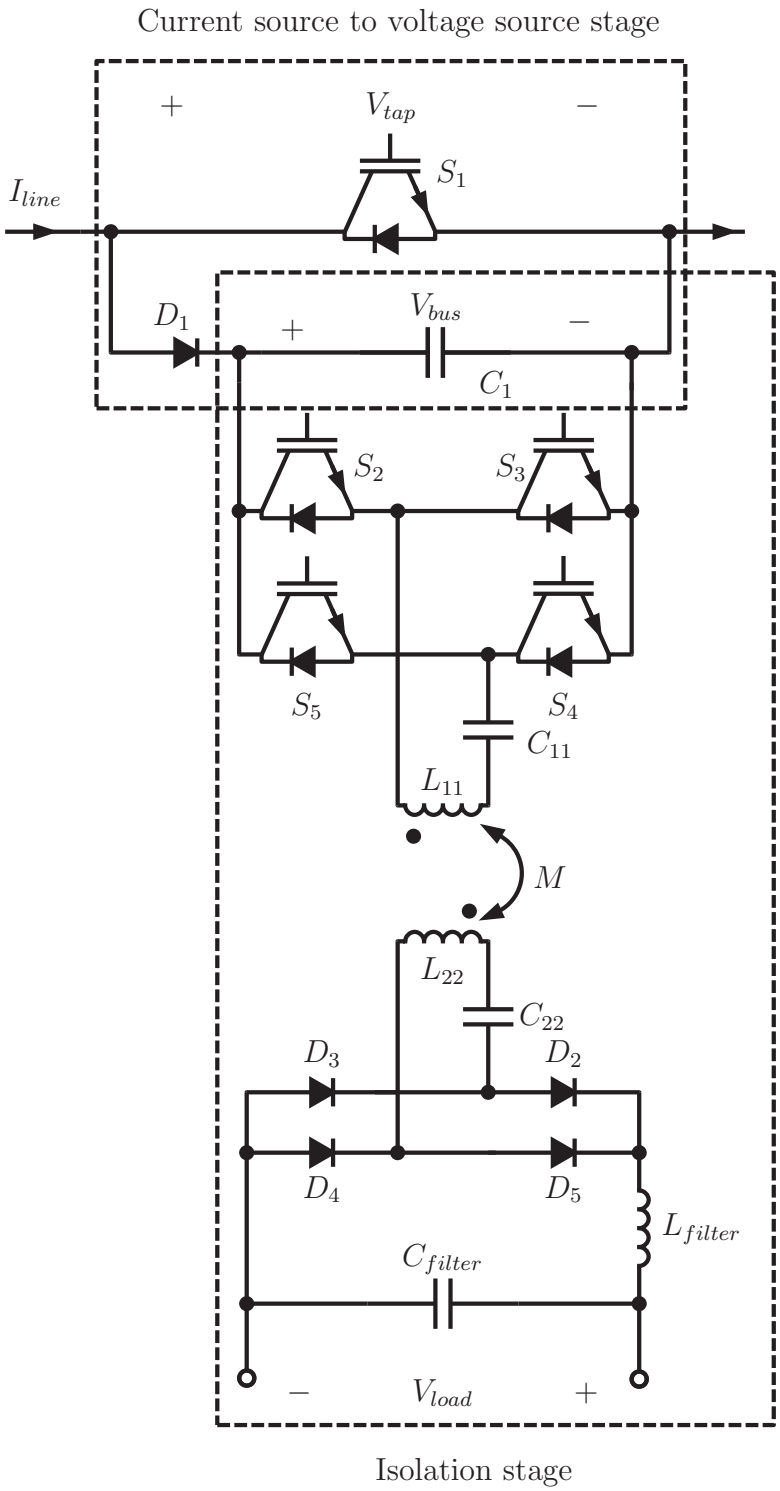

Figure 8.1 – Proposed Topology

compensated by series capacitors. The air-core transformer will then have a minimum impedance at the resonant frequency, allowing maximum power transfer at that frequency. Therefore, the full bridge will switch at the resonant frequency. The formulas for the compensation calculations are explained in Section 8.2.2. The output of the transformer is then rectified by a diode bridge and filtered by an inductor and capacitor. The output voltage will be under control, thereby forming a voltage source.

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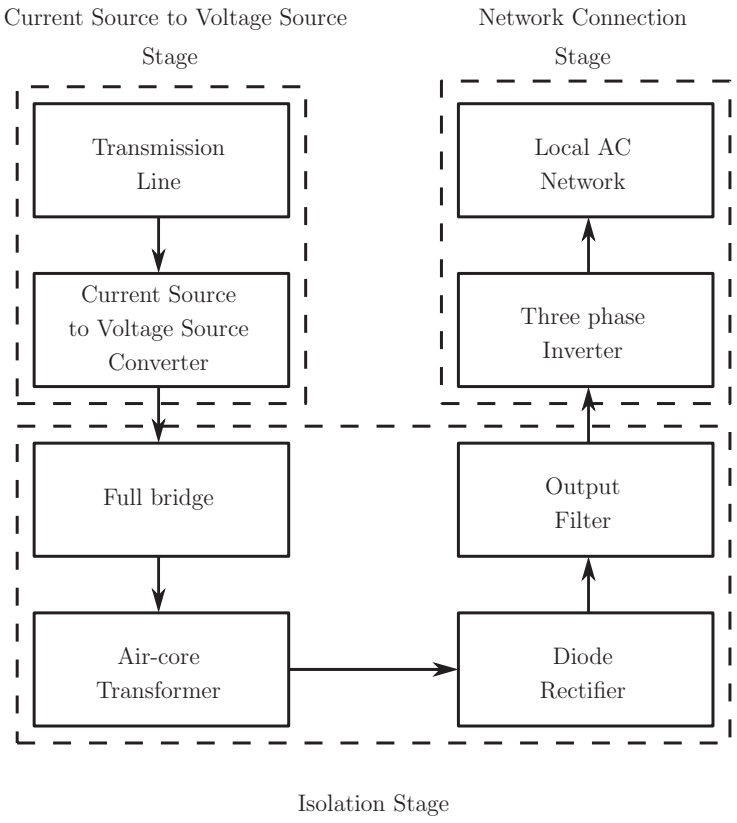

Figure 8.2 – Block Diagram

The last stage is the network connection stage. This stage converters the output voltage of the previous stage to the local AC network with the use of a three phase inverter. The design of the three phase inverter is beyond the scope of this thesis and will not be discussed. The output voltage of the three phase inverter may be stepped-up through a transformer to be able to connect to the local AC network.

The design of the current source to voltage source converter and the isolation converter will be subsequently discussed.

8.2.1 Current source to Voltage source stage analysis

The first part functions as a current source to voltage source converter. The line is modelled as a current source because of the large inductance of the line and the current mode control implemented at the rectifier of the HVDC transmission line. A capacitor is charged to a required voltage and regulated by a control circuit. Therefore a voltage source is created. Figure 8.3 shows the circuit diagram of the converter topology. For the analysis for this stage of the topology, the load resistance is connected across the bus capacitor.

This stage has two switching states. These states are referred to as the on and off state, respectively. In the on-state the switch S_1 is conducting. Conversely, the switch S_1 is in the non-conducting state during the off-state. The two states of the topology is shown in Figure

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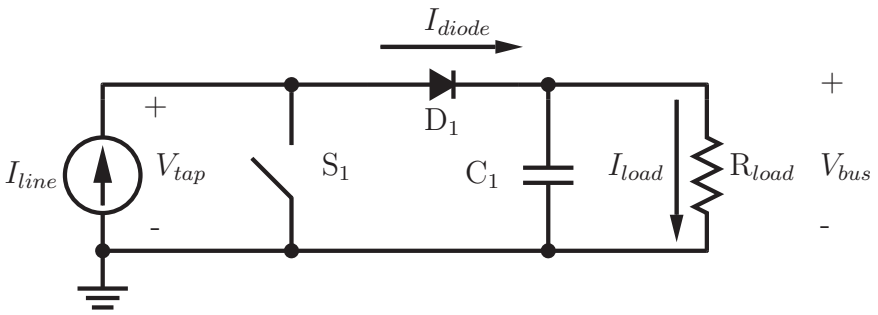

Figure 8.3 – Circuit Diagram of Topology

8.4 and 8.5. During the calculations, it is assumed that there are no losses and that the output voltage (V_{bus}) has a negligible ripple voltage.

The first state is defined to be the state while S_1 is in its conducting state, thus the on-state. Figure 8.4 shows the circuit diagram of the on-state.

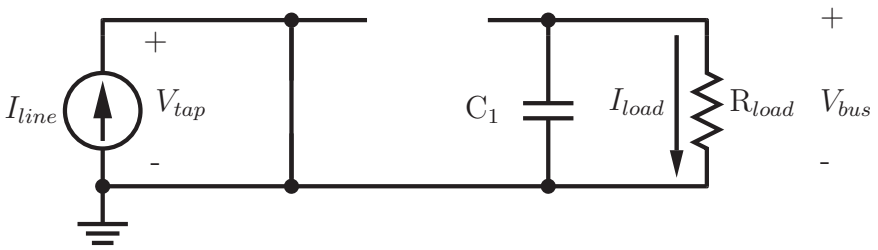

Figure 8.4 – Circuit Diagram of On-state

The second state is defined to be the state while S_1 is in its non-conducting state, therefore the off-state. Figure 8.5 shows the circuit diagram for the on-state.

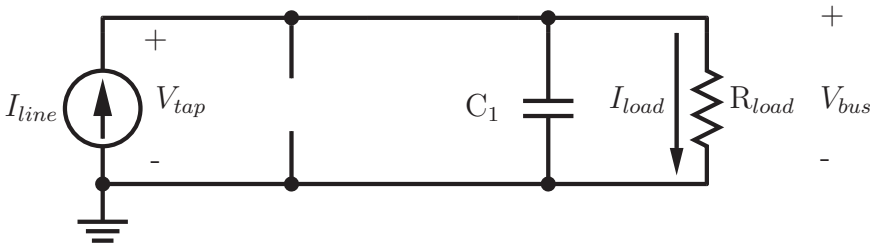

Figure 8.5 – Circuit Diagram of Off-state

In order to calculate the input power (P_{in}) and output power (P_{out}), the current I_{diode} needs to be determined. Figure 8.6 shows the current waveform of I_{diode}.

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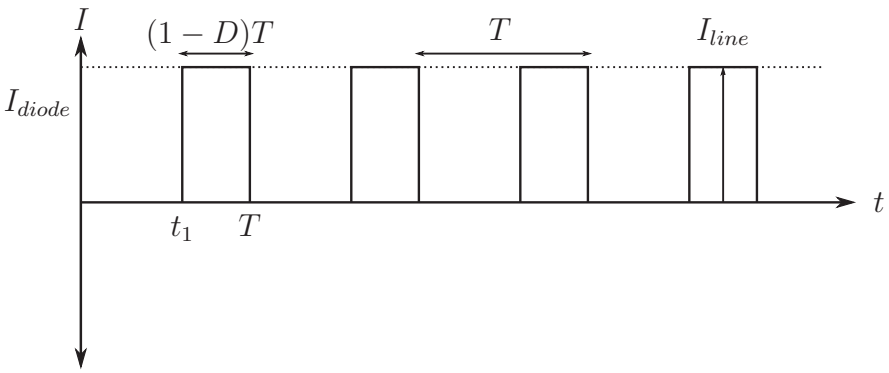

Figure 8.6 – I_{diode} Current Waveform

The average input power of the circuit is determined by calculating the average of the product of the current delivered by the current source (I_{line}) and voltage that appears across the current source (V_{tap}). The result is given by Equation 8.2.1.

$$\begin{aligned}
P_{in} &= \frac{1}{T}\int_0^T (I_{line})(V_{tap})\,\mathrm{d}t \\
&= \frac{1}{T}\Big(\int_0^{t_1} (I_{line})(0)\,\mathrm{d}t + \int_{t_1}^T (I_{line})(V_{bus})\,\mathrm{d}t\Big) \\
&= \frac{1}{T}\Big(0 + \int_{t_1}^T (I_{line})(V_{bus})\,\mathrm{d}t\Big) \\
&= \frac{1}{T}\Big[(I_{line}V_{bus})t\Big]_{t_1}^T \\
&= \frac{1}{T}\Big[(I_{line}V_{bus})(T) - (I_{line}V_{bus})(DT)\Big] \text{ with } t_1 = DT \\
&= (I_{line}V_{bus}) - (I_{line}V_{bus})(D) \\
&= (I_{line})(V_{bus})(1-D)
\end{aligned} \tag{8.2.1}$$

The output power of the circuit is given as the product of the square of the RMS load current (I_{load}) and the load resistance (R_{load}). In the case of a DC current, the mean and the RMS values are equal. The load current is the average of the diode current (I_{diode}). The load current is given by the Equation 8.2.2.

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$$\begin{aligned}
I_{load} &= \frac{1}{T}\int_0^T (I_{diode}(t))\,\mathrm{d}t \\
&= \frac{1}{T}\Big(\int_0^{t_1} (I_{diode}(t))\,\mathrm{d}t + \int_{t_1}^T (I_{diode}(t))\,\mathrm{d}t\Big) \\
&= \frac{1}{T}\Big(0 + \int_{t_1}^T (I_{line})\,\mathrm{d}t\Big) \\
&= \frac{1}{T}\Big[(I_{line})t\Big]_{t_1}^T \\
&= \frac{1}{T}\Big[(I_{line})(T) - (I_{line})(DT)\Big] \text{ with } t_1 = DT \\
&= (I_{line}) - (I_{line})(D) \\
&= (I_{line})(1-D) \qquad (8.2.2)
\end{aligned}$$

Subsequently, the average output power is calculated. The result is shown in Equation 8.2.3

$$\begin{aligned}
P_{out} &= (I_{load})^2 R_{load} \\
&= \Big((I_{line})(1-D)\Big)^2 R_{load} \qquad (8.2.3)
\end{aligned}$$

Assuming there are no losses, the input power is equal to the output power as shown in Equation 8.2.4. By substituting Equations 8.2.1 and 8.2.3 into 8.2.4 and making the duty cycle (D) the subject, Equation 8.2.5 is obtained.

$$\begin{aligned}
P_{in} &= P_{out} \qquad (8.2.4) \\
(V_{bus})(I_{line})(1-D) &= \Big((I_{line})(1-D)\Big)^2 R_{load} \\
V_{bus} &= (I_{line})(1-D)R_{load} \\
D &= 1 - \frac{V_{bus}}{I_{line}R_{load}} \qquad (8.2.5)
\end{aligned}$$

The allowable resistance can be derived by using the limits of duty cycle D.

$$\begin{aligned}
0 \;&<\; D \;<\; 1 \\
0 \;&<\; 1 - \frac{V_{bus}}{I_{line}R_{load}} \;<\; 1 \\
-1 \;&<\; \frac{V_{bus}}{I_{line}R_{load}} \;<\; 0 \\
1 \;&>\; \frac{V_{bus}}{I_{line}R_{load}} \;>\; 0 \\
\frac{I_{line}}{V_{bus}} \;&>\; \frac{1}{R_{load}} \;>\; 0
\end{aligned}$$

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$$R_{load} > \frac{V_{bus}}{I_{line}} \tag{8.2.6}$$

The Inequality 8.2.6 shows that the load resistance needs to be larger than $\frac{V_{bus}}{I_{line}}$.

8.2.2 Isolation stage analysis

The second part is a converter that drives the air-core transformer. As mentioned in Section 5.4.2, the air-core transformer provides the required isolation between the line- and earth-potential. Figure 8.7 show the circuit diagram for this stage.

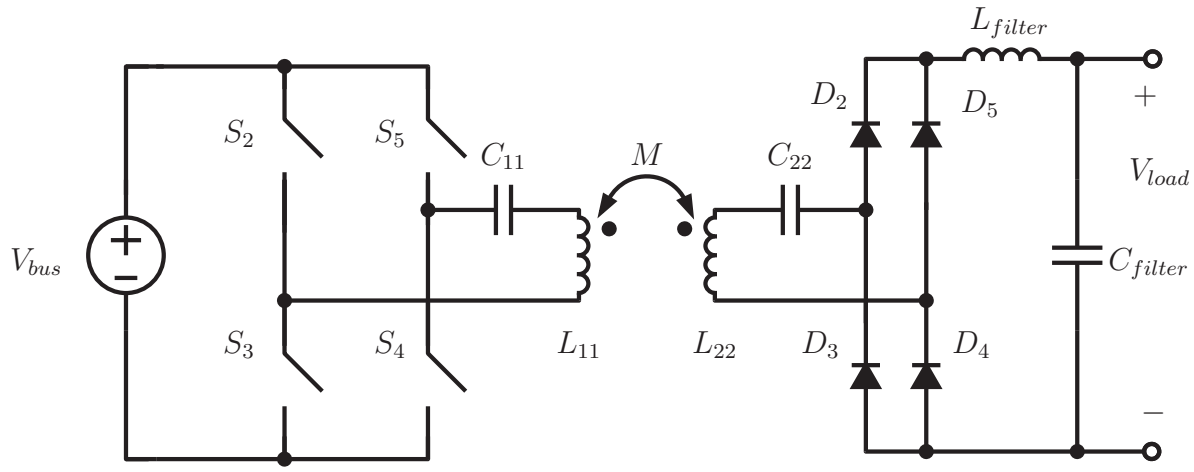

Figure 8.7 – Isolation Stage

The concept of the isolation stage is to compensate the self- and mutual inductances of the air-core transformer with series capacitors. The resonant frequency of the circuit will designed to be at the switching frequency of the full bridge.

The first part of the design concerns the choice of the switching frequency. This choice will affect the switching losses of the switches and the size required for the capacitors. The switching losses and the size of the required capacitances has a inverse proportional relationship. Therefore, a high switching frequency will have increased switching losses but will require capacitors with lower capacitances. In turn, larger capacitors will result in an increase in the cost. The switching frequency (f_s) will be chosen as low as the available capacitors will permit.

The switching frequency will be chosen as the resonant frequency of the series LC circuit. The capacitor needs to compensate for the entire inductance present in the air-core transformer. Figure 6.1 in Chapter 6 shows the equivalent circuit for an air-core transformer. The total inductance on the primary side is the sum of the self-inductance L_1 and the mutual inductance M. On the secondary side, the total inductance present is the sum of the self-inductance L_2 and the mutual inductance M.

The value for the capacitors is given by the Equations 8.2.7 and 8.2.8.

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$$C_{11} = \frac{1}{(2\pi f_s)^2(L_{11} + M)} \tag{8.2.7}$$

and

$$C_{22} = \frac{1}{(2\pi f_s)^2(L_{22} + M)} \tag{8.2.8}$$

A diode rectifier will rectify the current on the secondary and will be filtered by a bus cap, once again creating a bus voltage that will be used to power a three phase inverter. The three phase inverter will be used to connect to the local AC network.

8.3 Simulation Results

In this Section, a simulation demonstrating the operation of the analysed topology is presented. The same simulation parameters from Chapter 5 is used, although the results will be discussed in more detail. Simulation is performed in Simplorer 12. Figure 8.8 shows a screenshot of the workspace in Simplorer 15.

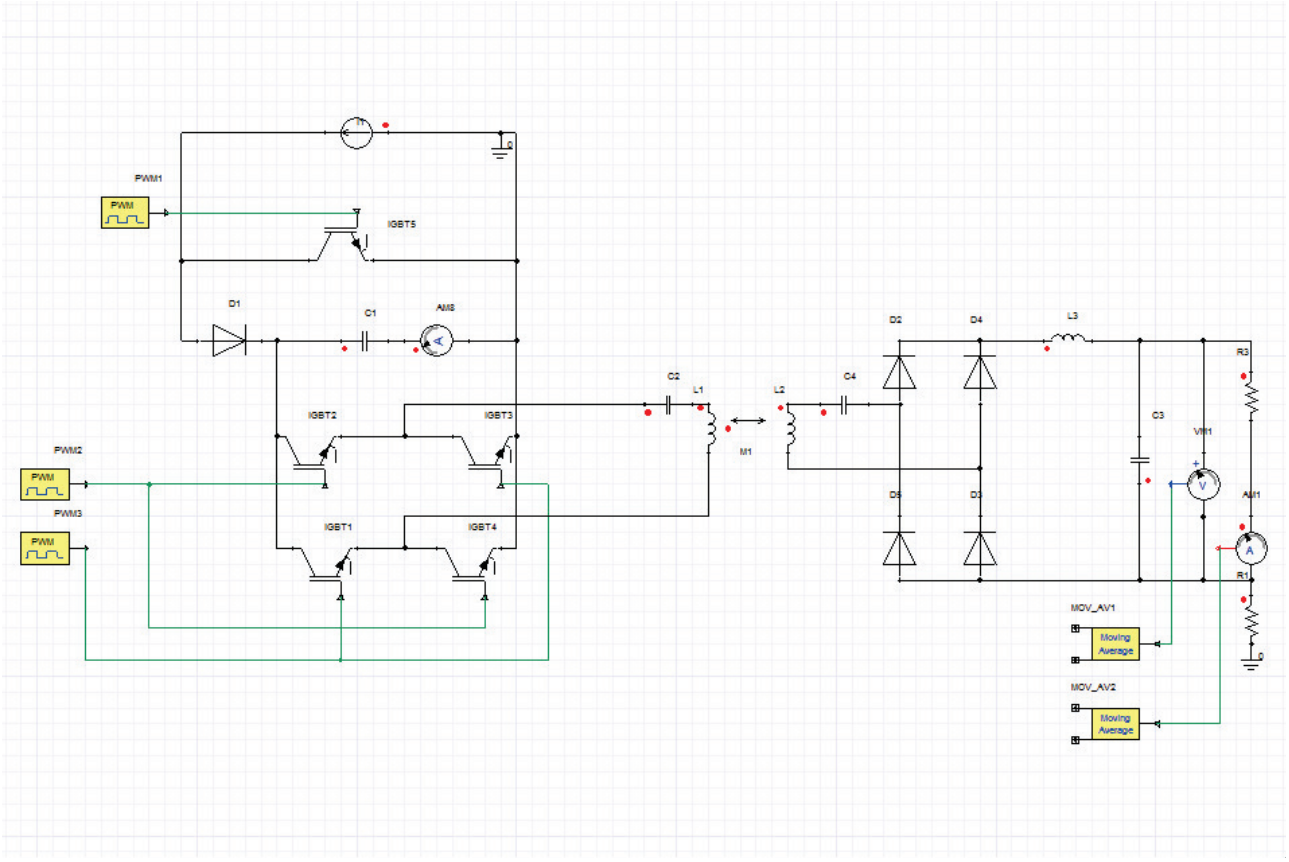

Figure 8.8 – Simplorer 15 Workspace Screenshot

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Table 8.1 contains the simulation parameters for the simulation performed. The results will be subsequently discussed. In all Figures, the grey trace shows the instantaneous value and the black trace indicates the average value as calculated by the simulation with an averaging period of 20 ms.

Figures 8.9 and 8.10 shows the voltage V_{bus}. It is important to note the small voltage ripple present.

The voltages that appear across the primary and secondary terminals of the compensated transformer is shown in Figure 8.11. The voltage V_{pri} is the sum of the voltage across the capacitor C_{11} and inductor L_{11}. The voltage V_{sec} is the sum of the voltage across the capacitor C_{22} and inductor L_{22}. Figure 8.12 shows the current in each of the windings of the transformer. These currents are I_{L11} and I_{L22}.

Figure 8.13 shows the voltages that appears across the compensation capacitors C_{11} and C_{22}. The maximum voltage across C_{11} is 130 kV and across C_{22} is 25 kV.

T_{end}	1000 ms
Timestep (min)	1 μs
Timestep (max)	10 μs
I_L	1800 A
C_1	10 mF
C_{11}	1.69 μF
C_{22}	42.22 μF
L_{11}	15 mH
L_{22}	0.6 mH
M	2.25 mH
L_{filter}	1 mH
C_{filter}	10 μF
f_s	1 kHz
D_{S1}	0.565

Table 8.1 – Simulation Parameters

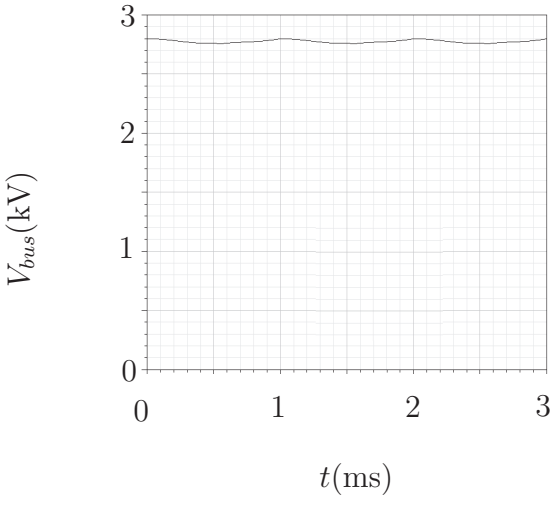

Figure 8.9 – V_{bus} Voltage

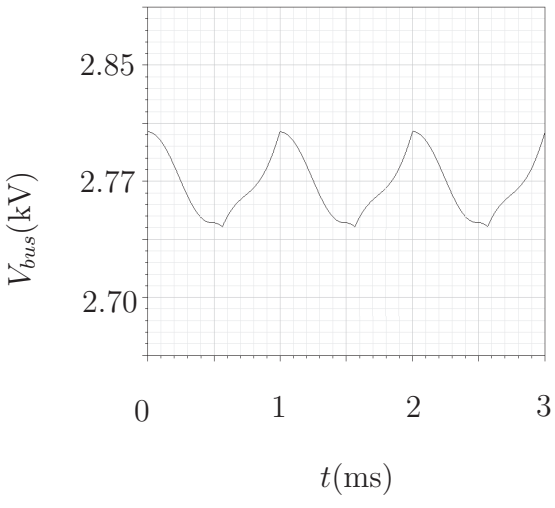

Figure 8.10 – V_{bus} Voltage - Enlarge

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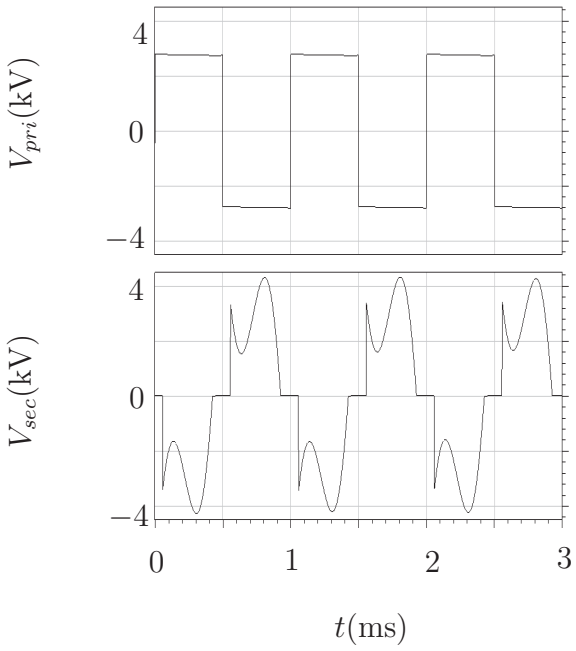

Figure 8.11 – Transformer Voltages

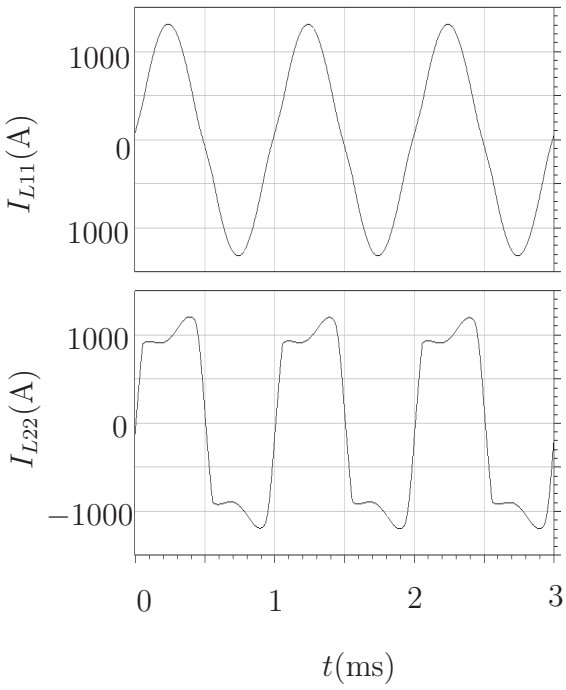

Figure 8.12 – Transformer Currents

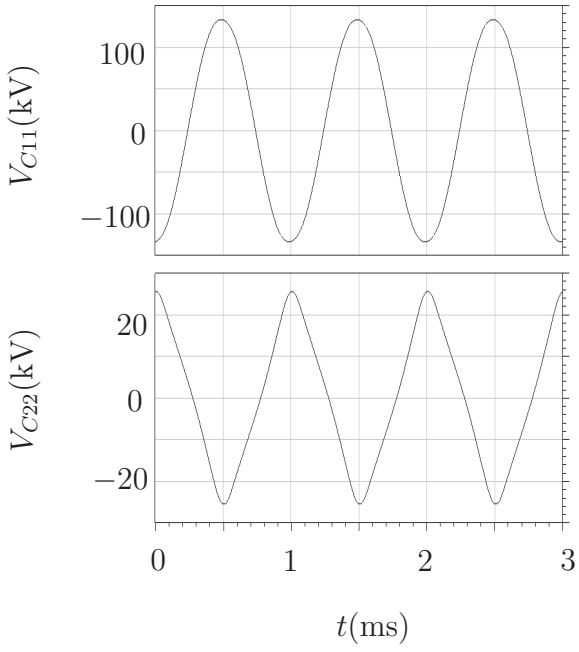

Figure 8.13 – Compensation Capacitor Voltages - V_{C11} & V_{C22}

As stated in Section 5.2, the developed series tap must deliver 2 MW at a bus voltage of 2 kV. Therefore the load current must be 1 000 A. Figures 8.14, 8.15, 8.16 and 8.17 show the transient simulation results. A resistive load is used in the simulation.

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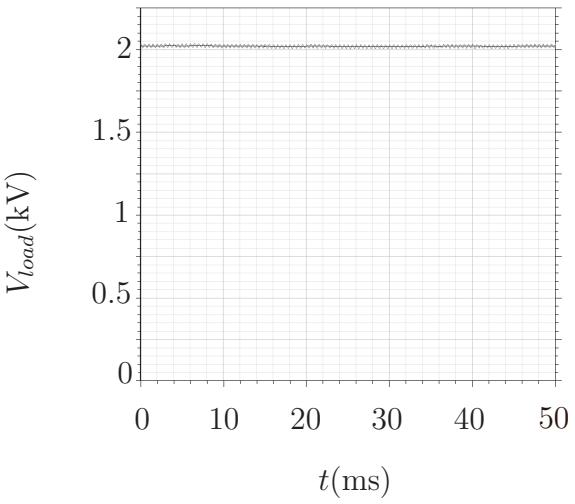

Figure 8.14 – Load Voltage

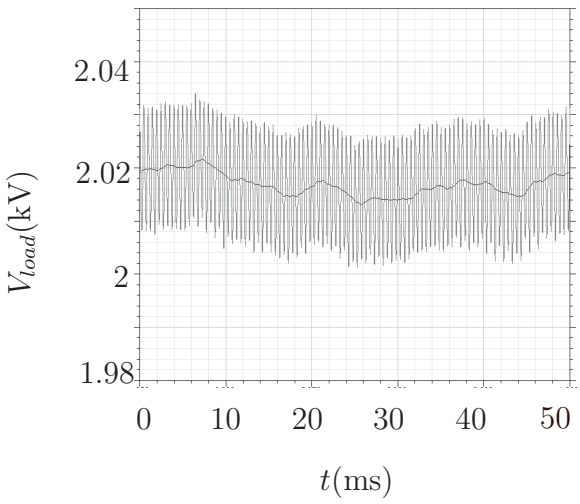

Figure 8.15 – Load Voltage - Enlarge

Figure 8.14 shows the load voltage. The simulated average load voltage is 2.025 kV. A ripple voltage of 50 V peak-to-peak is observed. The load current is shown in Figure 8.16. An average load current of 1 020 A is observed with a ripple current of 20 A peak-to-peak.

Using the average load current and average load voltage values from the simulation, the average power delivered to the resistive load is calculated to be 2.066 MW. The ripple voltage 2.46 % of the average load voltage and the ripple current is 1.96 % of the average load current. The ripple voltage and the ripple current will have a negligible effect on the three stage inverter stage that will be connected instead of the resistive load.

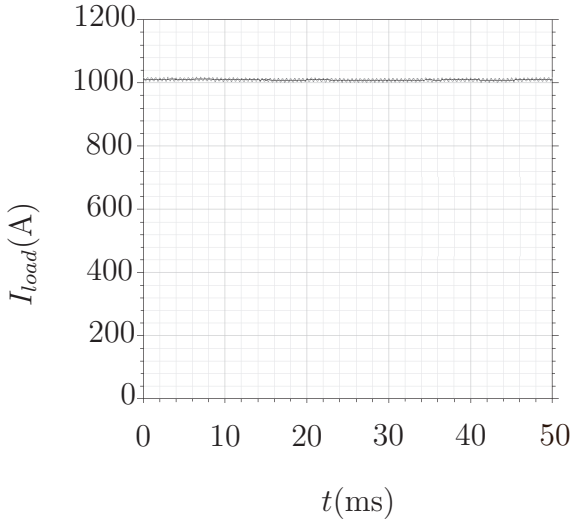

Figure 8.16 – Load Current

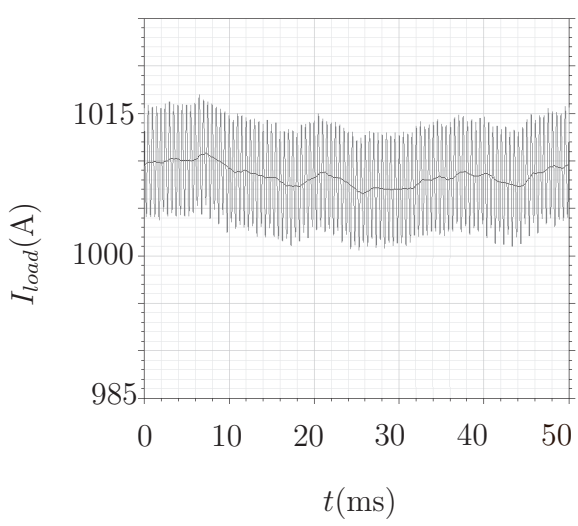

Figure 8.17 – Load Current - Enlarge

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The maximum voltage that appears across switch S_1 and diode D_1 is 2.77 kV and the maximum current is 1800 A. The switches S_2 to S_5 experience a maximum voltage of 4.30 kV and a maximum current of 1196.11 A. The diodes D_2 to D_5 in turn experience a maximum voltage of 2.76 kV and a maximum current of 1319.37 A. These voltages and currents are much lower than the voltages and currents that appear in the topology analysed in Chapter 7. Therefore, the topology analysed in this Chapter will be cheaper to construct and therefore a practical model will be constructed of this topology in the next Chapter.

8.4 Summary

This chapter discussed the second series tapping option proposed in Chapter 5. First, the derivation of the design equations was performed. Then a simulation was performed and the results were discussed. In the next Chapter, the design equations will be used to design a Series Tap Model.

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Chapter 9

Construction Of Series Tap Model

9.1 Introduction

This chapter describes the design and construction of a model of the HVDC Series tap topology investigated in Chapter 8. The model will serve as a proof of concept.

The design method analysed in Chapter 8 is used. The simulation described Chapter 6 provides the model for the air-core transformer that will be used in the model.

The chapter concludes with results when the HVDC Series Tap model is integrated into the HVDC Terminals Model that was designed and constructed in Chapter 3 and 4.

The specifications of the HVDC Series Tap model will be determined so that it will have the same power- and current rating ratios as found between the Cahora-Bassa HVDC Transmission System and the proposed series tap topologies, as specified in Chapter 5.

The power rating of the proposed taps are 2 MW, while the power rating of a single pole of the Cahora-Bassa HVDC Transmission System is 960 MW. The rating of the HVDC Terminals Model is 1 350 W. Therefore, to prove the operation, the HVDC Series Tap is required to deliver at least 2.8 W.

The load current of the proposed tap is 1 000 A and the line current of the Cahora-Bassa HVDC Transmission System is 1 800 A. Given that the line current of the HVDC Terminals Model is 3 A, the output current of the HVDC Series Tap model (I_{model}) is specified to be 1.7 A. Using the power and current specifications, the resistive load connected to the HVDC Series Tap model (R_{model}) is calculated to be 0.97 Ω but will be implemented as 1 Ω. Using the output current and resistive load values, the output voltage of the HVDC Series Tap model (V_{model}) is calculated to be 1.7 V. The required delivered power (P_{model}) with the specified output voltage and output current will be 2.89 W. It is more than the calculated minimum required delivered

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power and is therefore an acceptable specification. The HVDC Series Tap model is deemed as successful if the delivered power is equal or more than the required delivered power.

The design and implementation of a control loop for the HVDC Series Tap model is beyond the scope of this thesis.

9.2 Design, Simulation & Implementation

The objective of the tap model is to deliver power (P_{model}) to a resistive load (R_{model}). The design process starts with the design of the current source to voltage source converter stage and the isolation stage. The output voltage of the current source to voltage source converter is therefore assumed to be the same as the output voltage of the HVDC Series Tap (V_{out}). During the implementation stage, the duty cycle of the current source to voltage source converter will be adapted to compensate for the power losses present in the isolation stage. The switching frequency for both stages are the same and is defined as $f_{model} = 20\,\text{kHz}$.

After the both stages have been designed, the HVDC Series Tap model will be simulated in Simplorer 15. Simulation measurements are used to select appropriate components and consequently the thermal design is performed. A bypass switch is implemented using a relay. The relay driver is designed to have a 5 V logic input is designed so that the HVDC Series Tap model be controlled by a microcontroller.

Figure 9.1 shows the block diagram of the practical implementation of HVDC Series Tap model. The circuit diagram shown Chapter 5 is shown in Figure 9.2. The voltage and component designators have been adapted for the designed performed in this Chapter.

9.2.1 Current Source to Voltage Source Converter Stage Design

As stated in Chapter 3, the line current (I_{line}) is designed to be 3 A.

The calculated value for R_{model} needs to be varied by checking if the value satisfies Inequality 8.2.6. Since the calculated value for R_{model} satisfied Inequality 8.2.6, as seen in Inequality 9.2.1, it is shown that the value is valid.

$$\begin{aligned} R_{load} &> \frac{V_{model}}{I_{line}} \\ 1 &> 0.33 \end{aligned} \tag{9.2.1}$$

Using Equation 8.2.5 from Chapter 8, the duty cycle of the current source to voltage source converter (D_{model}) that will deliver the required amount of power can be calculated. The result is shown in Equation 9.2.2.

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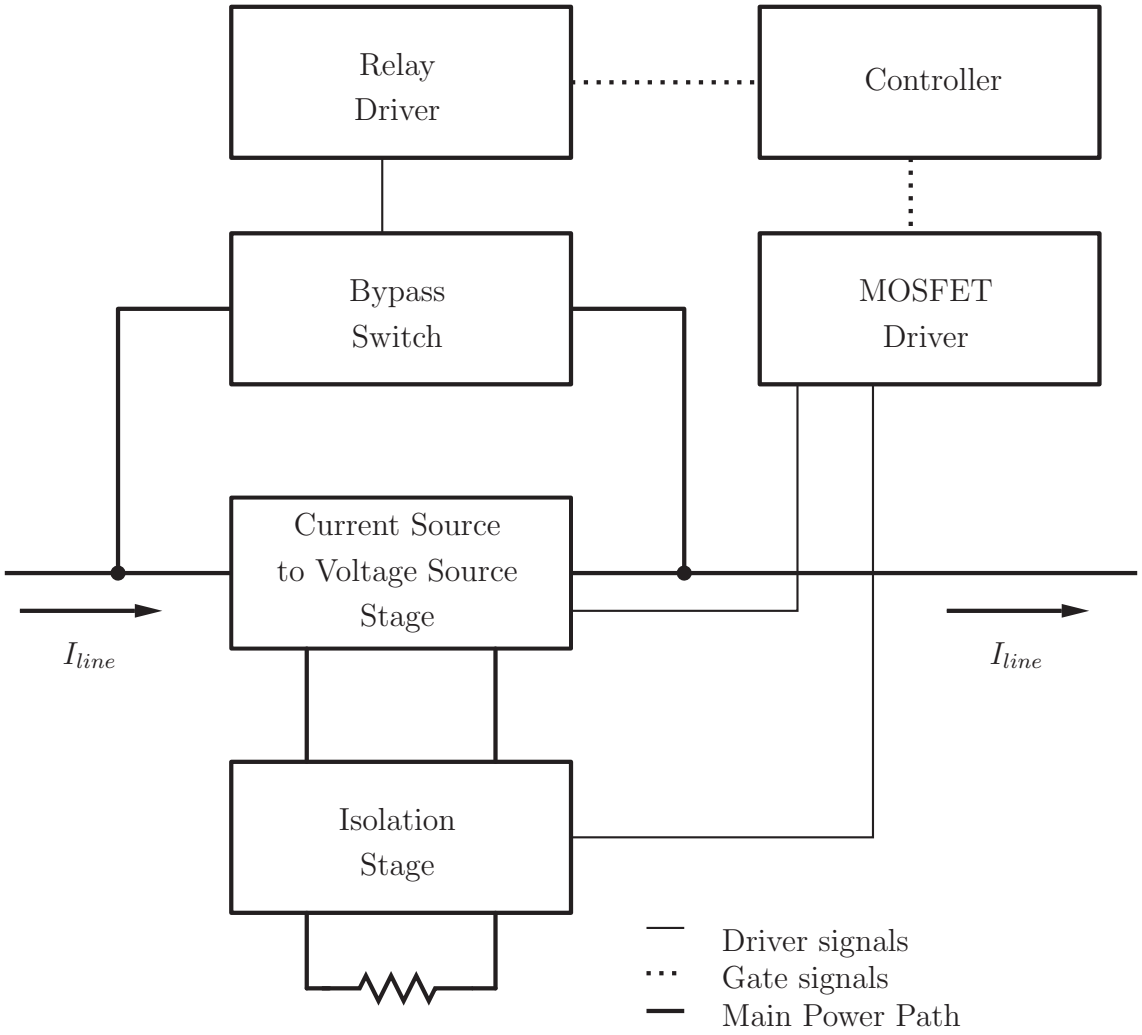

Figure 9.1 – Functional Block diagram of the HVDC Series Tap Model

$$D_{model} = 1 - \frac{V_{model}}{I_{line} R_{model}} = 0.43 \tag{9.2.2}$$

The bus capacitor (C_1) that forms part of the current source to voltage source converter stage is chosen to have a value of 1 mF. This choice of value is based on the availability of components.

9.2.2 Isolation Stage Design

The air-core transformer will have the same structure as the air-core transformer analysed in Chapter 6. The structure consists of a primary winding inside the secondary winding.

In order to design the compensation capacitors, the self- and mutual inductances must determined. The self-inductances of the two windings can be directly measured using an appropriate

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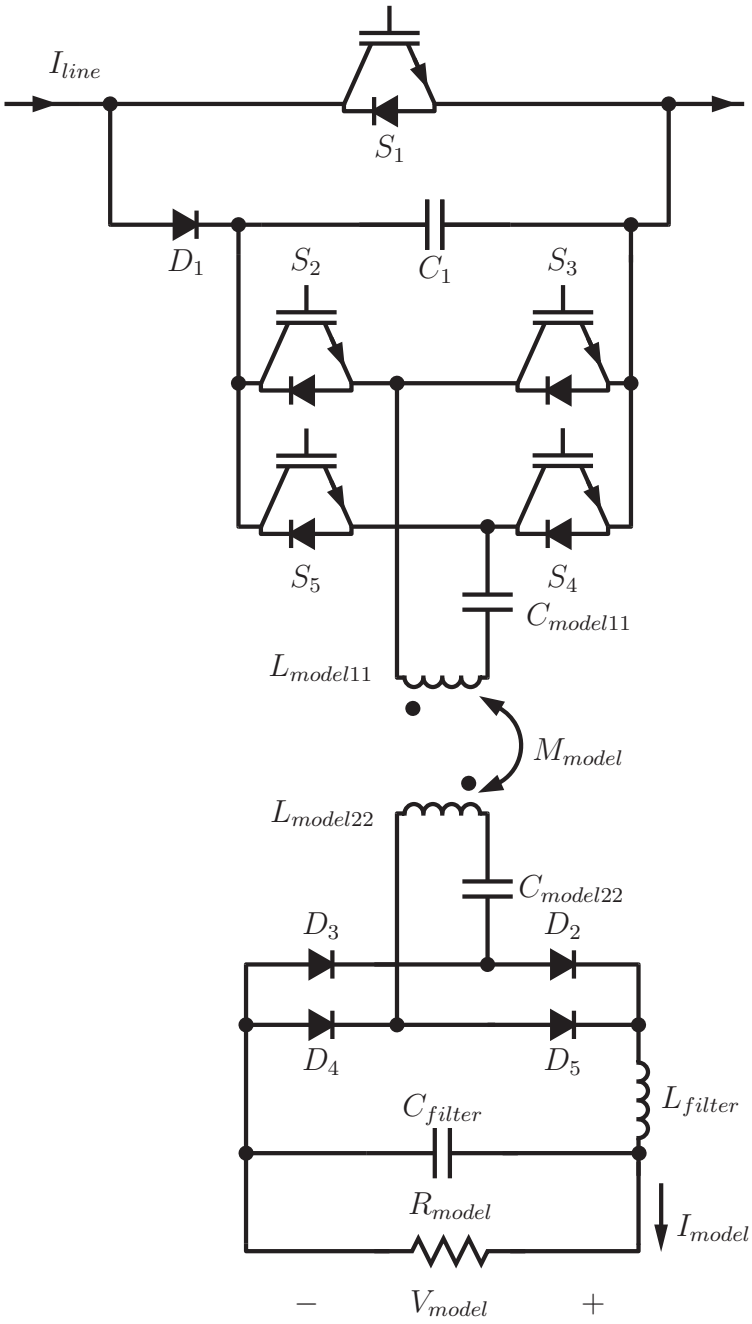

Figure 9.2 – Circuit Diagram of the HVDC Series Tap Model

measurement device.

The isolation between the windings must at least be 1000 V. Insulation tape will be applied to provide the required isolation. The isolation between turns of a single winding will be provided by the enamel coating of the copper wire.

The primary- and secondary winding will consist of 10 turns each. The turns will be wound as close as possible to each other. The radius of the primary winding is 37 mm and the radius of the secondary winding is 39 mm. The pitch of both windings is 4 mm. Insulation between the windings are provided by the enamel coating of the copper wire.

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The isolation resistance was measured at 1 GΩ using a Insulation Resistance Tester. The isolation did not fail at a test voltage of 1000 V.

The inductances of the air-core transformer were measured to be $L_{model11} = 7.70\,\mu$H and $L_{model22} = 8.40\,\mu$H. The mutual inductance was determined by connecting the two windings in series, measuring the total inductance, subtracting the self-inductances and finally dividing by two. Subsequently, the mutual inductance was determined to be $M_{model} = 5.55\,\mu$H.

The values for the compensating capacitors ($C_{model11}$ and $C_{model22}$) were calculated using Equations 8.2.7 and 8.2.8 from Chapter 8. The result is shown in Equation 9.2.3 and 9.2.4.

$$\begin{aligned} C_{model11} &= \frac{1}{(2\pi f_{model})^2(L_{model11} + M_{model})} \\ &= 4.78\,\mu\text{F} \end{aligned} \tag{9.2.3}$$

and

$$\begin{aligned} C_{model22} &= \frac{1}{(2\pi f_{model})^2(L_{model22} + M_{model}))} \\ &= 4.54\,\mu\text{F} \end{aligned} \tag{9.2.4}$$

The output filter inductor (L_{filter}) is chosen to have a value of 1 mH and the output filter capacitor (C_{filter}) is chosen to have a value of 1 mH. This choice of values is based on the availability of components.

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9.2.3 Simulation

The values for the design above is simulated in Simplorer. Figure 9.3 shows the simulation workspace in Simplorer 15. The switches and diodes are modelled as ideal components. The air-core transformer only consists of inductor and therefore does not have any resistive losses.

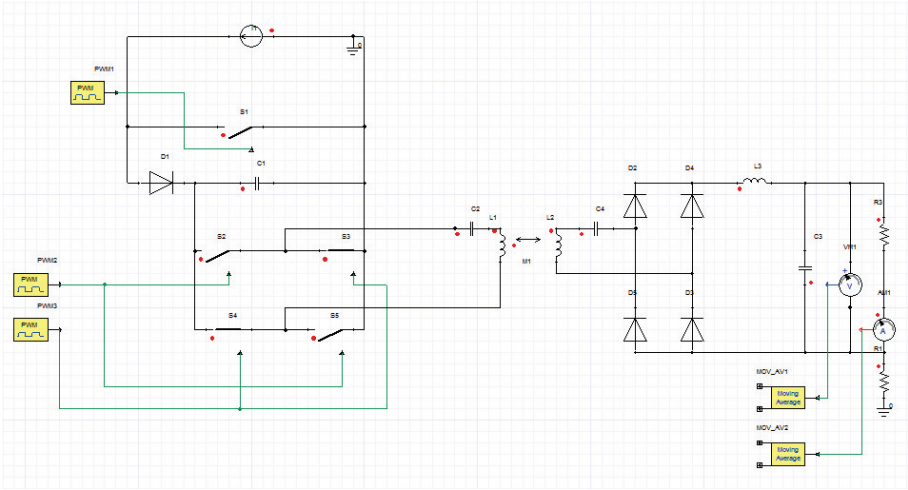

Figure 9.3 – Simplorer 15 Workspace Screenshot

Table 9.1 shows the simulation parameters used.

Figure 9.4 shows the simulated output current and Figure 9.5 shows the simulated output voltage. The output current (I_{model}) has a mean value of 1.72 A, while the output voltage has a mean value of 1.73 V. The delivered power is simulated to be 2.98 W. The required power is exceeded by 90 mW and therefore the simulation is successful in proving the designed values as feasible. Figures 9.4 and 9.5 includes the start-up transient from time 0 ms to 20 ms.

T_{end}	100 ms
Timestep (min)	1 μs
Timestep (max)	10 μs
I_L	3 A
C_1	1 mF
C_{11}	4.78 μF
C_{22}	4.53 μF
L_{11}	7.7 μH
L_{22}	8.4 μH
M	5.55 μH
L_{filter}	1 mH
C_{filter}	1 μF
f_s	20 kHz
D_{S1}	0.39

Table 9.1 – Simulation Parameters

9.2.4 Component Selection

From the simulation, the following components must be able to withstand the following voltages and currents. The switch S_1 must be able to withstand 4.10 V and 3 A. The diode D_1 has to be able to block 3.69 V and conduct 3 A. The switches S_2 to S_5 must have a voltage rating of at least 3.7 V and a current rating of 6.3 A. Lastly, the diodes must be able to withstand a voltage of 4.75 V and a current of 1.74 A.

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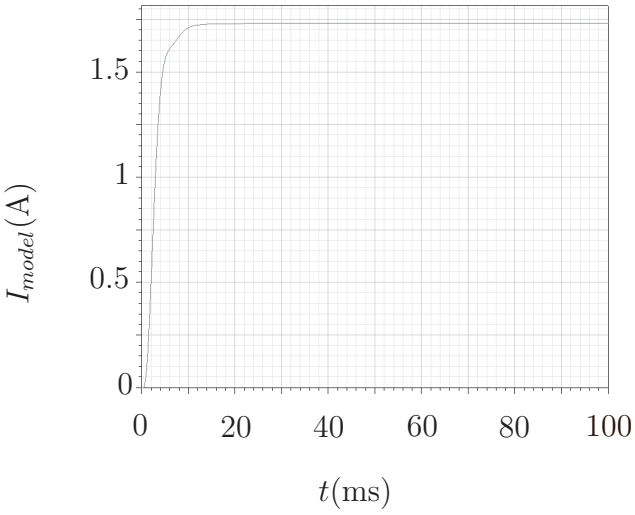

Figure 9.4 – Simulated I_{model}

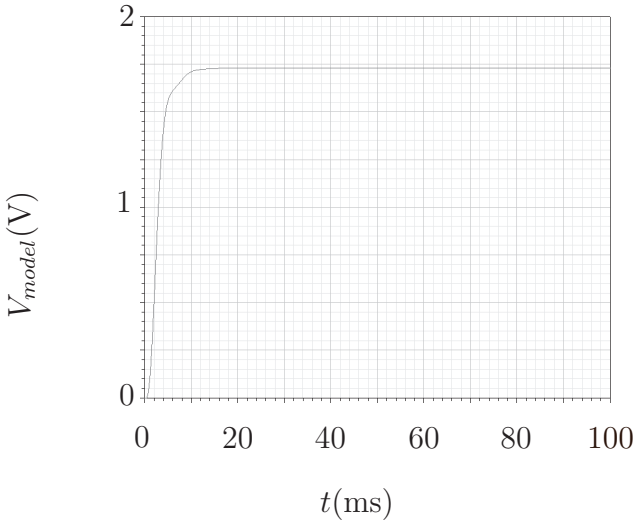

Figure 9.5 – Simulated V_{model}

The switching devices must have as little voltage drop across them as possible because the series tapping model will operate in the order of single volts. The devices that were considered for implementation are IGBTs and MOSFETs. IGBTs have a forward voltage across their collector and emitter terminals in the order of single volts. At such a low operating voltage, these devices would have a significant influence on the operation of the HVDC Series Tap model. MOSFET have an on-resistance in the order of tens of milli-ohms. At the rated line current of 3 A, the voltage drop across the drain and source terminals would be 30 mV per 10 mΩ. The voltage drop across the drain and source terminals would be insignificant. Therefore, MOSFETs would be best suited for the implementation of the switches (S_1 to S_5) of the HVDC Series Tap model. The STW20NM60 MOSFET is chosen for its high voltage rating and low on-resistance. The high voltage rating will provide increased reliability and an increased ability to withstand transient voltages during the start-up of the HVDC Terminals Model. The low on-resistance will allow for a low drain-source voltage and reduced losses. Reduced losses will allow the use of a smaller heat sink. These MOSFETs will be used in both stages of the HVDC Series Tap model.

The STTH1512 diode is chosen for the current source to voltage source converter stage diode (D_1) because of its high voltage rating and ultra fast operation. A voltage drop is expected between the input voltage and the output voltage of the isolation stage because of resistive losses in the air-core transformer, slight mismatch in the compensation capacitors and the forward voltage of the diode rectifier bridge. To keep the voltage drop as low as possible, diodes with the lowest possible forward voltage must be used. In light of this requirement, it is decided to use Schottky diodes because these diodes have very low forward voltages. The 1N5817 Schottky is chosen to be used in the diodes of rectifier bridge (D_2 to D_5) of the isolation stage.

The dsPIC33FJ16GS502 is chosen as the controller because of the versatile PWM module. The PWM module has a resolution of 1.04 ns and has several PWM outputs that can be

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individually configured. The gate signals for both the current source to voltage converter stage and the isolation stage can generated from this single processor.

A bypass switch will be used to bypass the series tapping model when the tap is not operational. A relay will be used to implement the bypass switch. The Omron G2RL-14 relay has a contact rating of 12 A.

9.2.5 Thermal Design

The MOSFETs S_1 to S_5 and the diode D_1 may require to be mounted on a heat sink to ensure reliable operation. The losses associated with each will of the aforementioned components will calculated and a thermal design will be performed.

It is assumed that the losses in a diode is predominantly conduction losses and therefore switching losses will be ignored. The losses in a diode (P_{D1}) is calculated by determining the product of the forward voltage ($V_{forward}$) and the average current through the diode (I_{D1}). Using the simulation in Section 9.2.3, the average current through diode $D1$ is calculated as 1.86 A using the simulation. The forward voltage is obtained using its component datasheet. Consequently, the losses is calculated and the result is shown in Equation 9.2.5.

$$\begin{aligned} P_{D1} &= V_{forward}\, I_{D1} \\ &= (1.2)(1.86) \\ &= 2.23\,\text{W} \end{aligned} \tag{9.2.5}$$

The losses of MOSFET S_1 is defined as P_{S1}. All of the other MOSFETs (S_2 to S_5) will have equal losses because they form a full-bridge that switches symmetrically. Only the losses of S_2 will be calculated and is defined as P_{S2}. The losses of a MOSFET comprises of switching losses ($P_{S1(swit)}$ and $P_{S2(swit)}$) and conduction losses ($P_{S1(cond)}$ and $P_{S2(cond)}$). Because a MOSFET has a on-resistance, the conduction losses of a MOSFET is the product of the square the RMS current through the MOSFET (I_{S1rms} and I_{S2rms}) and the on-resistance (R_{on}). The on-resistance is obtained using the component datasheet and is determined to be 0.26 Ω. As with the diode, the RMS current through the MOSFETs were calculated to be $I_{S1(rms)} = 1.85$ A and $I_{S2(rms)} = 2.69$ A using the simulation. Equation 9.2.6 and 9.2.7 shows the result.

$$\begin{aligned} P_{S_1(cond)} &= (I_{S1rms})^2 R_{on} \\ &= (1.85)^2(0.26) \\ &= 0.89\,\text{W} \end{aligned} \tag{9.2.6}$$

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$$\begin{aligned} P_{S_2(cond)} &= (I_{S2rms})^2 R_{on} \\ &= (2.69)^2(0.26) \\ &= 1.89\,\text{W} \end{aligned} \tag{9.2.7}$$

The switching losses of a MOSFET is calculated by determining the switching losses when switching on and off. The formula for calculating switching losses in given in [31]. Equation 9.2.8 show the formula for switching losses with t_{on} defined as the rise time of the MOSFET, t_{off} defined as the fall time of the MOSFET, V_{swit1} and I_{swit1}. The rise- and fall times were obtained using the component datasheet. The voltage V_{swit1} is assumed to be of the same magnitude as the voltage across C_1. This voltage is assumed to be 1.7 V. The current I_{swit1} is assumed to be of the same magnitude as the line current I_{line}. The result for the switching losses calculation for S_1 is shown in Equation 9.2.9. From the datasheet of the MOSFET, $t_{on} = 20\,\text{ns}$ and $t_{off} = 11\,\text{ns}$.

$$P_{S_1(swit)} = \frac{1}{2} t_{on} V_{swit1} I_{swit1} f_{model} + \frac{1}{2} t_{off} V_{swit1} I_{swit1} f_{model} \tag{9.2.8}$$

$$\begin{aligned} &= \frac{1}{2} V_{swit} I_{swit} f_{model} (t_{on} + t_{off}) \\ &= \frac{1}{2}(1.7)(3)(20\,000)(31\text{x}10^{-9}) \\ &= 1.58\,\text{mW} \end{aligned} \tag{9.2.9}$$

The MOSFETs forming the full-bridge (S_2 to S_5) drives the air-core transformer that is compensated with capacitors so that it act as a resonant circuit. Equation 9.2.10 shows the formula for $P_{S2(swit)}$ and the result given by Equation 9.2.11.

$$P_{S_2(swit)} = \frac{1}{2} t_{on} V_{swit2on} I_{swit2on} f_{model} + \frac{1}{2} t_{off} V_{swit2off} I_{swit2off} f_{model} \tag{9.2.10}$$

$$= 3.11\,\text{mW} \tag{9.2.11}$$

The total power losses for the MOSFET S_1 is given by Equation 9.2.12 and for MOSFETs S_2 to S_5 is given by Equation 9.2.13.

$$\begin{aligned} P_{S1} &= P_{S1(swit)} + P_{S1(cond)} \\ &= 891.58\,\text{mW} \end{aligned} \tag{9.2.12}$$

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$$\begin{aligned} P_{S2} &= P_{S3} = P_{S4} = P_{S5} \\ &= P_{S2(swit)} + P_{S2(cond)} \\ &= 1.893\,\text{W} \end{aligned} \tag{9.2.13}$$

All the MOSFETs will be mounted to the heat sinks. The MOSFET S_1 and diode D_1 will each be mounted on its own heat sink with a thermal resistance (θ_{s-a1}) of 24 °C/W. The MOSFETs S_2 and S_3 will be mounted on a heat sink with a thermal resistance (θ_{s-a2}) of 4.7 °C/W. The MOSFETs S_4 and S_5 will be mounted on another heat sink with the same thermal resistance as the previous heat sink. The junction to sink thermal resistances is dependent on the packages of the component. Diode D_1 has a TO-220 package and has a thermal resistance (θ_{j-c1}) of 1.3 °C/W. The MOSFETs have a TO-247 package and each has a thermal resistance (θ_{j-c2}) of 0.58 °C/W. The case to sink thermal resistance (θ_{c-s}) is assumed to be the same as in Chapter 3.

Figure 9.6 shows the equivalent thermal circuit.

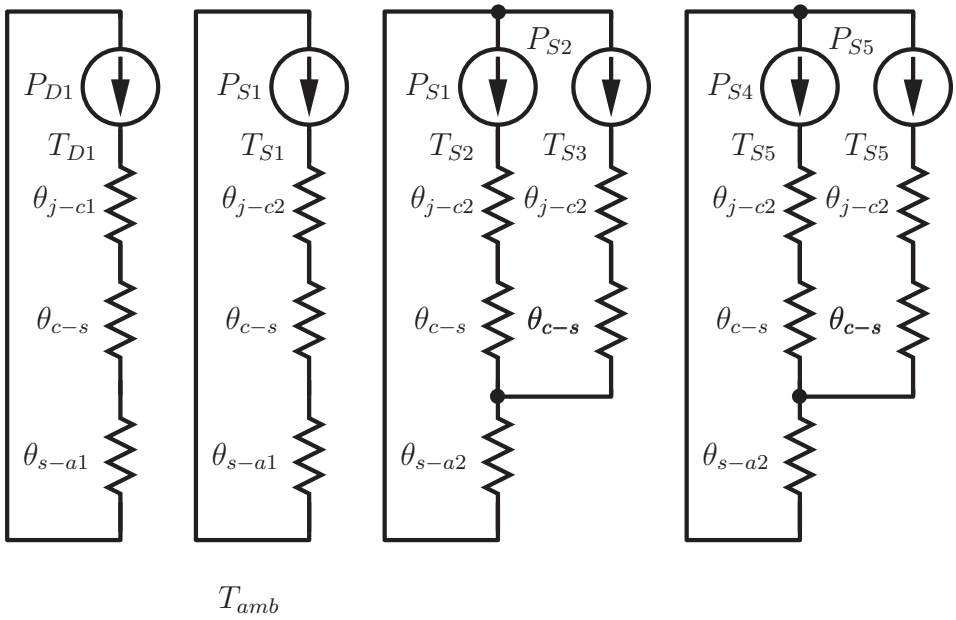

Figure 9.6 – Thermal Design

The junction temperatures of each above-mentioned component is calculated, assuming the ambient temperature is 30 °C. Table 9.2 shows the calculated results. Each component's junction temperature is within the operating specifications.

T_{D1}	86.87 °C
T_{S1}	52.09 °C
T_{S2}	49.24 °C
T_{S3}	49.24 °C
T_{S4}	49.24 °C
T_{S5}	49.24 °C

Table 9.2 – Thermal Design Results

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9.2.6 MOSFET drivers

In order to drive the MOSFETs, a voltage need to be applied between the gate and source terminals. This voltage needs to be galvanically isolated from other voltages that uses another ground. Therefore, floating voltage are required to drive each MOSFET that is not connected to the control circuit ground. The required floating voltages are provide by the use of the Mornsun B1215LS dc-dc converter. These floating voltages are then applied to the MOSFETs using the TLP250 driver integrated circuit. Gate signals are isolated through the opto-coupler included in the TLP250 driver.

The gate resistor (R_{gate}) is used to limit the current into the gate of the MOSFET (I_{gate}). By limiting the current, the turn-on time of the MOSFET is limited and damage to the gate of the MOSFET is prevented by excessive gate currents. Each MOSFET will have the same gate resistor. Figure 9.7 show the schematic for the MOSFET driver. The positive terminal of the gate voltage V_{gate} is connected to the gate terminal of the MOSFET and the negative terminal is connected to the source terminal of the MOSFET.

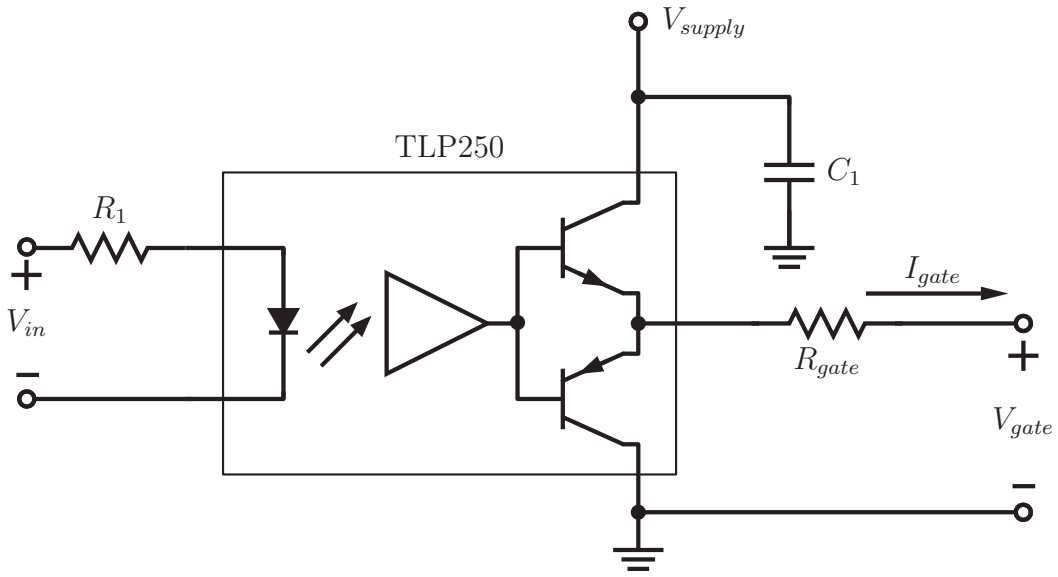

Figure 9.7 – MOSFET Driver

The resistor R_1 is used to bias the LED of the opto-coupler and the capacitor C_1 is used to filter the supply of the MOSFET driver.

The gate resistor is designed using the following method. The gate capacitance (C_{gate}) of the MOSFET is estimated using the estimation described in [65]. From the datasheet of the STW20NM60 MOSFET, the gate capacitance to be 35 pF. The rise time (T_{on}) of the MOSFET is determined to be 20 ns. The gate resistor and the gate capacitance forms a RC circuit with

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the time constant defined as $\tau = R_{gate}C_{gate}$. The time constant is taken to be the rise time. The result is shown in Equation 9.2.14.

$$\begin{aligned} R_{gate} &= \frac{\tau}{C_{gate}} \\ &= 571.42\,\Omega \end{aligned} \tag{9.2.14}$$

The gate resistor will be practically implemented with the standard value of 560 Ω.

The peak gate current is estimated using Equation 9.2.15 that is described in [66]. The internal gate resistance of the MOSFET ($R_{gate(int)}$) is obtained from the datasheet and is specified to be 1.6 Ω. The voltage $V_{gate(on)}$ is the voltage used to switch the MOSFET on and is equal to the supply voltage (V_{supply}) of the MOSFET driver and is 15 V. The threshold voltage of a MOSFET is a minimum gate-source voltage that needs to be applied before the MOSFET will start to switch on or off. This voltage is denoted as $V_{gate(th)}$ and is specified in the datasheet as 4 V. The results is given in Equation 9.2.16.

$$I_{gate(peak)} = \frac{V_{gate(on)} - V_{gate(off)}}{R_{gate} + R_{gate(int)}} \tag{9.2.15}$$

$$\begin{aligned} &= \frac{15 - 4}{560 + 1.6} \\ &= 19.59\,\text{mA} \end{aligned} \tag{9.2.16}$$

The peak gate current can be delivered without damaging the TLP250 MOSFET driver IC. The control signal V_{in} will be supplied from the controller.

9.2.7 Relay driver

A relay driver circuit is built to power the relay used as a bypass switch that can be controlled from a 5 V logic signal. The relay coil has a required current of 350 mA to operate the relay contacts. A MOSFET is used to switch the required current. A LED (D_1) is switched with the relay to be used a signal indicator and is biased with R_2. The resistor R_1 is used to bias the LED of the opto-coupler. The capacitor C_1 is used to filter the supply voltage of the relay driver $V_{supply2}$. A free-wheel diode (D_2) is included to avoid damage to the MOSFET caused by over-voltages caused by the interruption of the current flowing through the relay's coil.

Isolation between the switching circuit and the switching signal is provided by the use of the TLP250. The TLP250 is applied in the same manner as in the MOSFET driver. Figure 9.8 shows the schematic for the relay driver. The gate resistor (R_3)is designed using the same procedure as described in previous section.

In the practical implementation of the HVDC Series Tap model the control signal (V_{in}) to the relay driver is supplied by a manual switch.

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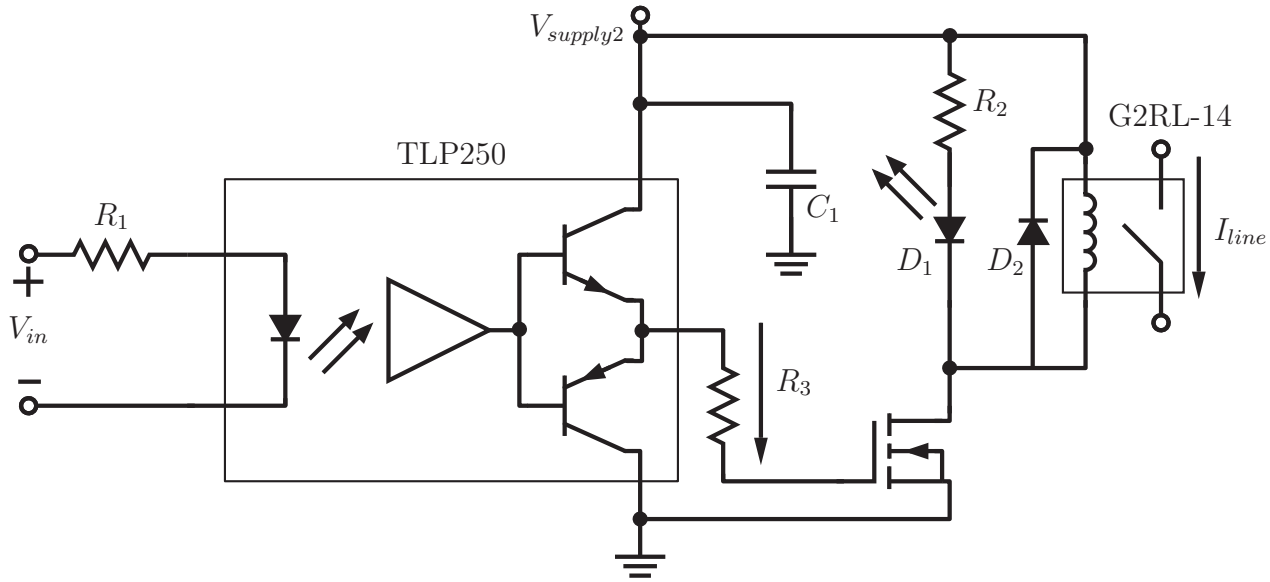

Figure 9.8 – Relay Driver

9.3 Results

Figure 9.9 shows the construction of the HVDC Series Tap model. The component designators refer to the definitions made in the circuit diagram of the HVDC Series Tap model in Figure 9.2. Table 9.3 shows the legend to the numbering in Figure 9.2.

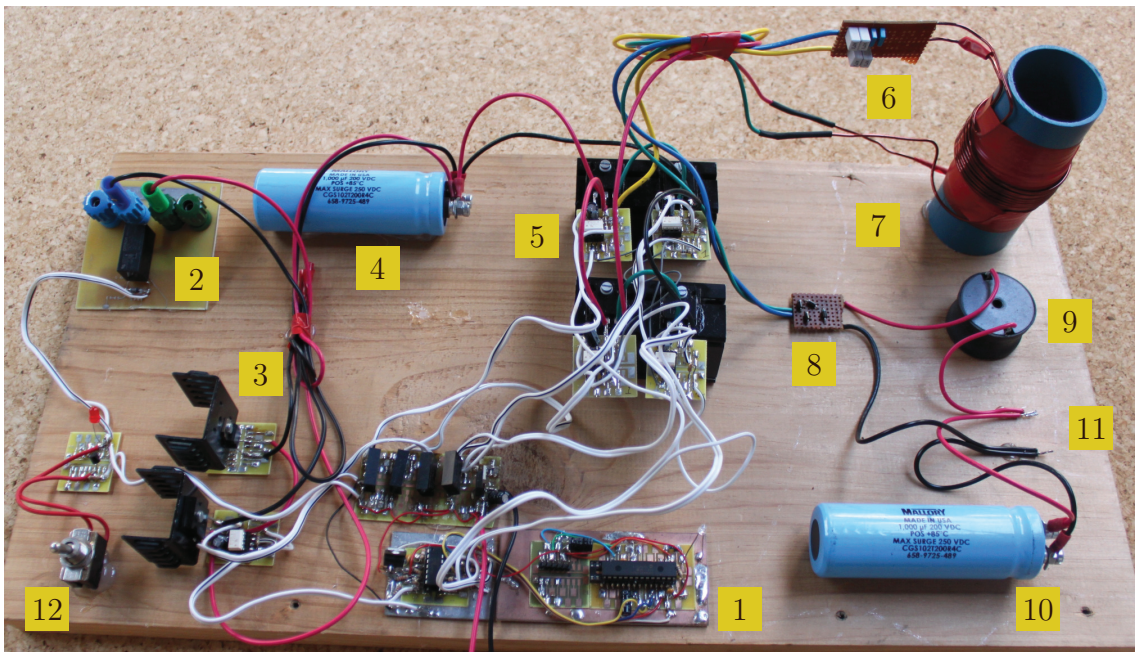

Figure 9.9 – HVDC Series Tap Model Construction

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The lower the duty cycle is inversely proportional to the output voltage. Therefore the duty cycle was lowered to 0.2 to accommodate the losses associated with the air-core transformer and component losses that were ignored during the design. . Figure 9.10 shows the measured results. The top trace shows the output voltage (V_{model}) and the bottom trace shows the output current (I_{model}) of the HVDC Series Tap model.

1	Controller
2	By-pass switch
3	Current source to voltage source converter stage
4	Capacitor C_1
5	Isolation Stage Full-bridge
6	Capacitors C_{11} & C_{22}
7	Air-core transformer
8	Isolation stage diode rectifier bridge
9	Filter Inductor L_{filter}
10	Filter Capacitor C_{filter}
11	Load Connection Terminals
12	HVDC Series Tap model control

Table 9.3 – HVDC Series Tap Model Legend

The mean value of V_{model} is measured to be 2.2 V. Similarly, the mean value of I_{model} is measured to be 1.65 A. Because both the voltage V_{model} and the current I_{model} are DC entities, and therefore the product can be used to calculate the power delivered. Using the product of these DC values, the total power that practically delivered (P_{model}) is calculated to be 3.63 W. The practical implementation of the HVDC Series Tap model delivers 0.74 W more than the target power of 2.89 W. The difference is subscribed to the change in the duty cycle.

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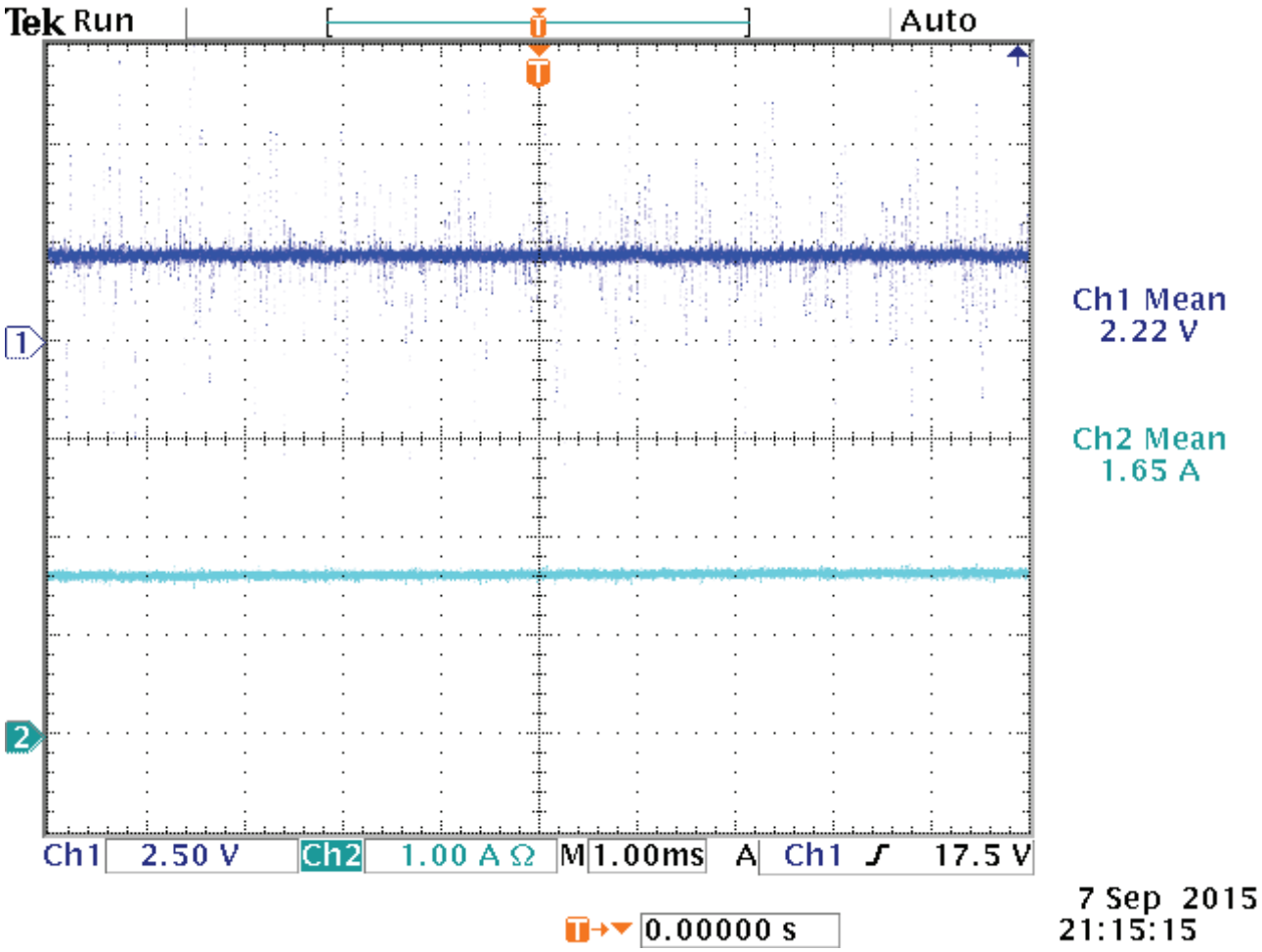

Figure 9.10 – Measured HVDC Series Tap Model Results

Because the HVDC Series Tap model successfully deliver more than the required amount of power to the load, it is concluded that adequate proof of concept is provided so that the HVDC Series Tap model can be implemented on a larger scale.

9.4 Summary

In this chapter the construction of the HVDC Series Tap Model is discussed. First, a design is performed so that the model will deliver 2.89 W to a resistive load. The design is then confirmed in simulation. Lastly, the practical implementation of the HVDC Series Tap Model connected to the HVDC Terminals Model is confirmed with measurements. It is found that the practical implementation of the HVDC Series Tap model deliver slightly more power than the design requirement because of a change in the duty cycle.

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Chapter 10

Conclusion

10.1 Overview

10.1.1 HVDC Transmission Line Model

Chapter 3 described the design, simulation and construction of the hardware used to construct the HVDC Transmission Line Model. Correct operation was confirmed by the use of practical measurements.

Chapter 4 documented the procedure used to design the controllers used for the Thyristor Rectifier and the Thyristor Inverter. The chapter showed how a transfer function for the thyristor converters are derived and how a PI controller is designed. The design was implemented on a FPGA.

10.1.2 Selection of appropriate a HVDC Series Tap topology

Chapter 5 investigated and compared the different power transfer techniques as possible solutions to tapping power from a HVDC Transmission Line. Mechanical, chemical and electrical options were considered. Two options using an air-core transformer were chosen to be further analysed.

Chapter 6 discussed the simulation developed to simulate an air-core transformer. The simulation provided the self-inductances of each of the windings and the mutual inductance between the windings. The chapter discusses electromagnetic theory used the numerical method used to calculate these properties of the air-core transformer. The chapter concluded with simulation results that showed the relation between physical description and the coupling factor.

Chapter 7 investigated the first HVDC Series Tap topology proposed in [17]. The operation of the tap was analysed, but it was recommended that another topology must be used for the HVDC Series Tap.

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Chapter 8 discussed and analysed the HVDC Series Tap topology proposed in [50]. Design equations were derived. The equation were confirmed in a full scale simulation of a HVDC series tap is completed. The topology was chosen that would be implemented as the HVDC Series Tap model.

10.1.3 Construction of HVDC Series Tap Model

Chapter 9 documented the design, simulation and construction of the HVDC Series Tap Model. The design was performed using the equations derived Chapter 8. The HVDC Series tap was successfully practically implemented with the HVDC Transmission Line model and the results were presented.

10.2 Recommendations and Future Work

10.2.1 HVDC Transmission Line Model

Different modern control techniques used elsewhere in power electronics can be investigated for application in HVDC converters. The performance of such controllers can be tested on the HVDC Transmission Line Model.

10.2.2 Air-core transformer

The simulation of the air-core transformer can be achieved by using more accurate integration methods and integrating over the spiral surface created by the air-core transformer.

The simulation can be extended to calculate the forces exerted by the windings on each other. This will aid in designing a full scale air-core transformer.

The simulation can also be extended to calculate the current density in the conductors of the windings. The skin effect and the proximity effect must be taken into account because of the high frequency used to drive the transformer and the presence of harmonics.

10.2.3 HVDC Series Tap

A HVDC Series Tap topology that allows for bi-directional power flow can be investigated. This ability will allow to extend the possible applications of a HVDC Series Tap in future. This can be achieved by reversing the polarity of the line capacitor. The tap would then add power to the HVDC transmission line. This tap can then be used to gather of scattered small generating plant, for example renewable generation.

The current topology introduces current and voltage harmonics on the HVDC transmission line. Harmonics on a HVDC transmission line will interfere with the control and protection systems installed on the line. It will also transmit electromagnetic interference. Reduction of

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harmonics will allow the tap to be implemented on older technology that is very susceptible to harmonics.

10.3 General Conclusions

Firstly, it was concluded that the HVDC Terminals model was successfully constructed. The correct amount of power was transmitted. Furthermore, controllers for both thyristor converters were implemented. This complete system created an environment where the HVDC Series Tap model could be tested.

The topology chosen for the construction of the HVDC Series Tap model was successfully constructed, tested and integrated with the HVDC Terminals model. The HVDC Series Tap model managed to successfully tap power from the HVDC Terminals model without disturbing the operation of the HVDC Terminals model.

Finally, it was concluded that the HVDC Series Tap model provided adequate proof of concept so that further research is recommended. A larger setup should be constructed to further investigate further development opportunities.

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Appendix A

Derivation of Differential Equations

Differential equations can be used to analyse the behaviour of each state of the topology in Chapter 7. Four state variables is chosen by the importance shown in the previous figures. These definitions are shown in Figure A.1. To limit the number of state variables, the output capacitor (C_3) is chosen as a constant voltage V_O. This is a valid assumption because of the large capacitance of the capacitor.

A state is defined when a change in the circuit is made by the switching on or off of a switch or a diode. Using the simulation from the previous section, six states are identified. Each state is analysed subsequently. An equivalent circuit for the air-core transformer is used to simplify the calculations. State 1 starts when the switches S_1 and S_2 are switched on.

A.0.1 Air-core Transformer Equivalent Circuit Derivation

An equivalent is used to solve the differential equations. Figure A.2 shows the definition of the circuit diagram for a air-core transformer shown in Chapter 6. The equations 6.2.2 and 6.2.3 are also given.

$$V_1 = L_1 \frac{di_1}{dt} + M \frac{di_2}{dt}$$
$$V_2 = L_2 \frac{di_2}{dt} + M \frac{di_1}{dt}$$

As indicated in the previous section, the bus capacitor is assumed to show the same behaviour as a voltage source. Figure A.3 shows the voltage source added to the model. The polarity of the voltage will depend on the diodes conducting during a given state.

From Equation 6.2.3, substitute V_O for V_2 :

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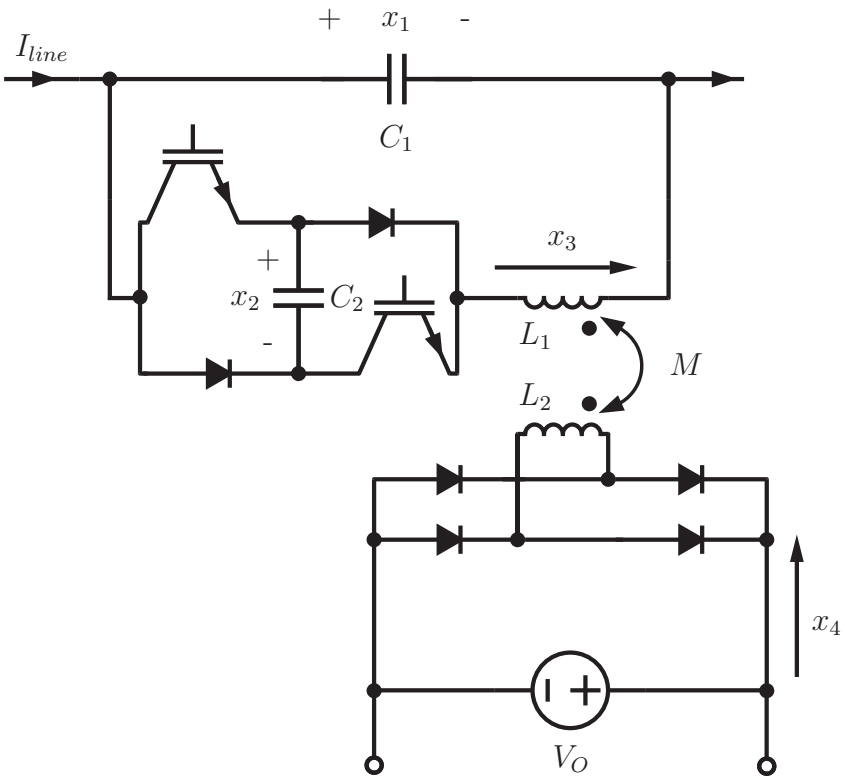

Figure A.1 – Definition of State Variables

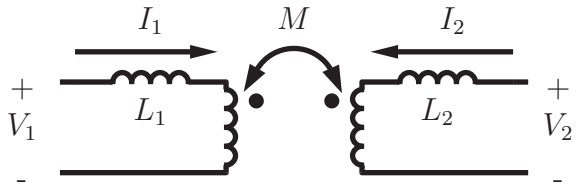

Figure A.2 – Definition of Air-core transfomer

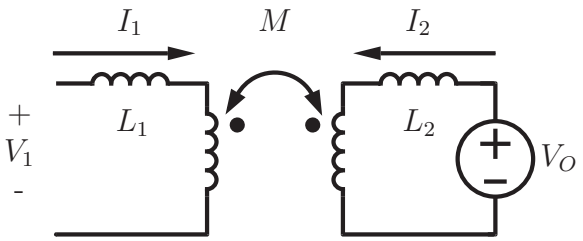

Figure A.3 – Definition of Air-core Transfomer

$$\frac{di_2}{dt} = \frac{1}{L_2}[V_O - M\frac{di_1}{di_2}] \tag{A.0.1}$$

Substitute Equation A.0.1 in Equation 6.2.2

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$$V_1 = L_1\frac{di_1}{dt} + \frac{M}{L_2}[V_O - M\frac{di_1}{di_2}]$$
$$= [L_1 - \frac{M^2}{L_2}]\frac{di_1}{dt} + \frac{M}{L_2}V_O \quad \text{(A.0.2)}$$

From Equation A.0.2, the equivalent circuit looks as in Figure A.4.

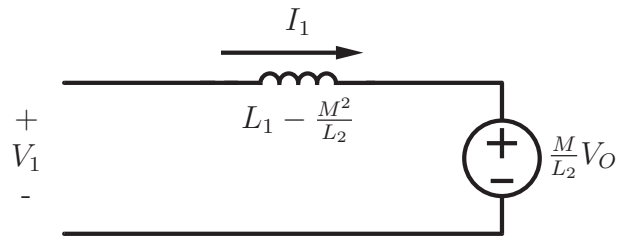

Figure A.4 – Definition of Air-core transfomer

This equivalent circuit is used throughout the derivation of the differential solutions of the different states.

A.0.2 State 1

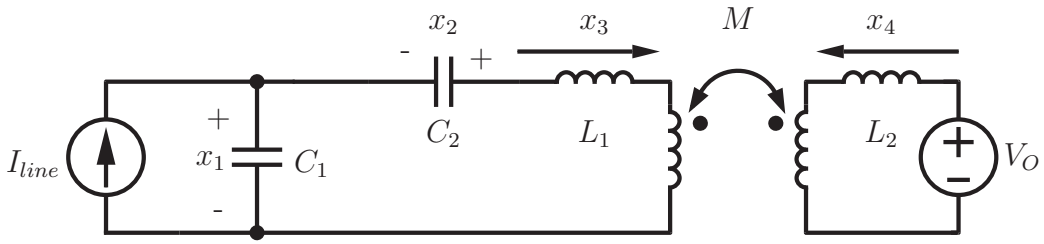

Figure A.5 – State 1 Circuit Diagram

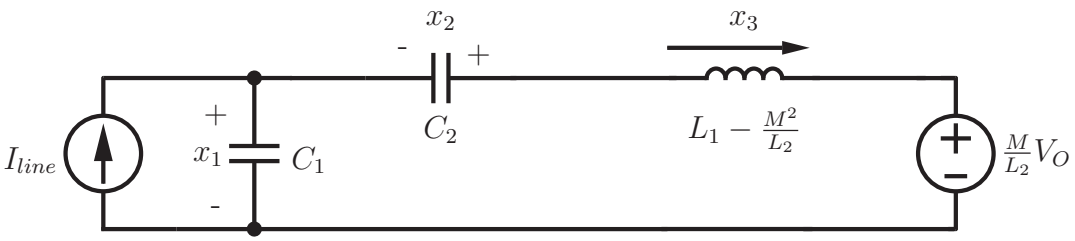

Figure A.6 – State 1 Equivalent Circuit Diagram

Equations obtained from equivalent circuit:

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$$I_L = C_1\dot{x}_1 + x_3 \tag{A.0.3}$$
$$x_3 = C_2\dot{x}_2 \tag{A.0.4}$$
$$0 = x_1 - x_2 - \gamma\dot{x}_3 - \frac{M}{L_2}V_O \tag{A.0.5}$$

with

$$\gamma = \left[L_1 - \frac{M^2}{L_2}\right]$$

Re-arrange Equation A.0.3, A.0.4 & A.0.5 to obtain:

$$\dot{x}_1 = \frac{-1}{C_1}x_3 + \frac{1}{C_1}I_L \tag{A.0.6}$$
$$\dot{x}_2 = \frac{1}{C_2}x_3 \tag{A.0.7}$$
$$\dot{x}_3 = \frac{1}{\gamma}x_1 - \frac{1}{\gamma}x_2 - \frac{M}{\gamma L_2}V_O \tag{A.0.8}$$

To solve x_3:
The solution to x_3 is found by differentiating Equation A.0.8 and solving the resulting differential equation. By differentiation, the following equation obtained:

$$\begin{aligned}\ddot{x}_3 &= \frac{1}{\gamma}[\dot{x}_1 - \dot{x}_2] \\ &= \frac{1}{\gamma}\left[\frac{1}{C_1}(I_L - x_3) - \frac{1}{C_2}x_3\right] \\ &= \left[\frac{-1}{\gamma C_1} + \frac{-1}{\gamma C_2}\right]x_3 + \frac{1}{\gamma C_1}I_L \\ &= -\alpha x_3 + \frac{1}{\gamma C_1}I_L \end{aligned} \tag{A.0.9}$$

with α defined as:

$$\alpha = \left[\frac{1}{\gamma C_1} + \frac{1}{\gamma C_2}\right]$$

Equation A.0.9 is a ordinary linear non-homogeneous differential equation. In order to find a general solution to the equation the homogene solution must first be found. The non-homogene solution, also known as a particular solution, must then be found. Because the differential equation is linear, the general solution can be obtained by adding the homomgene and non-homogene solutions and calculating the values of the integration constants.

Homogene solution:

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To find the homogene solution, the non-homogene part is set to zero. Equation A.0.10 is then obtained:

$$\ddot{x}_3 + x_3\alpha = 0 \tag{A.0.10}$$

This differential equation can be solved by substituting $x_3 = e^{mt}$, $\dot{x}_3 = me^{mt}$ and $\ddot{x}_3 = m^2e^{mt}$. Equation A.0.11 is then obtained by the following derivation:

$$\begin{aligned} m^2e^{mt} + \alpha e^{mt} &= 0 \\ e^{mt}\left(m^2 + \alpha\right) &= 0 \\ m^2 + \alpha &= 0 \end{aligned} \tag{A.0.11}$$

Solutions to Equation A.0.11 are given as:

$$\begin{aligned} m_1 &= j\sqrt{\alpha} \\ m_2 &= -j\sqrt{\alpha} \end{aligned}$$

By substituting and adding the different solutions of Equation A.0.11 into the $x_3 = e^{mt}$, the homogene solution is found.

$$x_3 = k_1e^{m_1t} + k_2e^{m_2t}$$

The constants k_1 and k_2 will be complex conjugates because the m_1 and m_2 are complex conjugates. To simplify the expression, the constants can then be redefinied as $k_1 = k$ and $k_2 = \bar{k}$. Therefore the homogene solution is given by:

$$x_3 = ke^{j\sqrt{\alpha}t} + \bar{k}e^{-j\sqrt{\alpha}t} \tag{A.0.12}$$

Particular solution:
To find a particular solution, Equation A.0.9 is evaluated at $\ddot{x}_3 = 0$.

$$\begin{aligned} \ddot{x}_3 + x_3\alpha &= \frac{I_L}{C_1\gamma} \\ 0 + x_3\alpha &= \frac{I_L}{C_1\gamma} \\ x_3 &= \frac{I_L}{\alpha\gamma C_1} \end{aligned} \tag{A.0.13}$$

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Test result:

$$0 + \alpha\left(\frac{I_L}{\alpha\gamma C_1}\right) = \frac{I_L}{\gamma C_1}$$
$$\frac{I_L}{\gamma C_1} = \frac{I_L}{\gamma C_1}$$

Therefore the result is valid.

General solution:

General solution is the sum of Equations A.0.12 and A.0.13

$$x_3 = ke^{j\sqrt{\alpha}t} + \bar{k}e^{-j\sqrt{\alpha}t} + \frac{I_L}{\alpha\gamma C_1} \tag{A.0.14}$$

To calculate k:

at $t = 0$ with $k = a + jb$:

To calculate a, evaluate Equation A.0.14 at $t = 0$ with the initial condition as $x_3 = x_3(0)$.

$$x_3 = ke^{j\sqrt{\alpha}t} + \bar{k}e^{-j\sqrt{\alpha}t} + \frac{I_L}{\alpha\gamma C_1}$$
$$x_3(0) = 2a + \frac{I_L}{\alpha\gamma C_1}$$
$$a = \frac{1}{2}\left[x_3(0) - \frac{I_L}{\alpha\gamma C_1}\right]$$

To calculate b. Evaluate A.0.8 at $t = 0$ with initial conditions defined as $x_1 = x_1(0)$ and $x_2 = x_2(0)$. The following equation is obtained:

$$\dot{x}_3 = \frac{-\frac{M}{L2}V_O + x_1(0) - x_2(0)}{\gamma} \tag{A.0.15}$$

By differentiating Equation A.0.14, the following result is obtained:

$$\dot{x}_3 = kj\sqrt{\alpha} - \bar{k}j\sqrt{\alpha} \tag{A.0.16}$$

By setting Equation A.0.15 equal to Equation A.0.16 and evaluating the resulting equation at $t = 0$, the following result is obtained:

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$$kj\sqrt{\alpha} - \bar{k}j\sqrt{\alpha} = \frac{-\frac{M}{L2}V_O + x_1(0) - x_2(0)}{\gamma}$$

$$k - \bar{k} = \frac{-\frac{M}{L2}V_O + x_1(0) - x_2(0)}{j\sqrt{\alpha}\gamma}$$

$$2jb = \frac{-j\left[-\frac{M}{L2}V_O + x_1(0) - x_2(0)\right]}{\sqrt{\alpha}\gamma}$$

$$b = \frac{-x_1(0) + x_2(0) - \frac{M}{L2}V_O}{2\sqrt{\alpha}\gamma}$$

Therefore x_3 is given by:

$$x_3 = ke^{j\sqrt{\alpha}t} + \bar{k}e^{-j\sqrt{\alpha}t} + \frac{I_L}{\alpha\gamma C_1}$$

with $k = \left(\frac{1}{2}\left[x_3(0) - \frac{I_L}{\alpha\gamma C_1}\right]\right) + j\left(\frac{x_1(0) - x_2(0) + \frac{M}{L2}V_O}{2\sqrt{\alpha}\gamma}\right)$

To obtain the other state variable solutions, the integral of x_3, defined as β, must be calculated.

$$\beta = \frac{k}{j\sqrt{\alpha}}e^{j\sqrt{\alpha}t} + \frac{\bar{k}}{-j\sqrt{\alpha}}e^{-j\sqrt{\alpha}t} + \frac{I_L t}{\alpha\gamma C_1} + \delta$$

with δ as the integration constant.

The integral should be equal to zero at time equals. Therefore: $\beta = 0$ for $t = 0$.
To calculate δ, set $\beta = 0$ and $t = 0$.

$$\begin{aligned}
\beta &= \frac{k}{j\sqrt{\alpha}}e^{j\sqrt{\alpha}t} + \frac{\bar{k}}{-j\sqrt{\alpha}}e^{j\sqrt{\alpha}t} + \frac{I_L t}{C_1\alpha\gamma} + \delta \\
0 &= \frac{k}{j\sqrt{\alpha}} + \frac{\bar{k}}{-j\sqrt{\alpha}} + \delta \\
\delta &= \frac{k}{j\sqrt{\alpha}} + \frac{\bar{k}}{-j\sqrt{\alpha}} \\
&= \frac{-(a+jb)}{j\sqrt{\alpha}} + \frac{(a-jb)}{j\sqrt{\alpha}} \\
&= \frac{-2b}{\sqrt{\alpha}}
\end{aligned}$$

Therefore β is the given by:

$$\beta = \frac{k}{j\sqrt{\alpha}}e^{j\sqrt{\alpha}t} + \frac{\bar{k}}{-j\sqrt{\alpha}}e^{j\sqrt{\alpha}t} + \frac{I_L t}{C_1\alpha\gamma} + \frac{-2b}{\sqrt{\alpha}}$$

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To obtain x_1:

Substitute the expression for β into Equation A.0.6 and by integration the following solution is found:

$$x_1 = \frac{I_L t}{C_1} - \frac{1}{C_1}\left[\frac{k}{j\sqrt{\alpha}}e^{j\sqrt{\alpha}t} + \frac{\bar{k}}{-j\sqrt{\alpha}}e^{-j\sqrt{\alpha}t} + \frac{I_L t}{\alpha\gamma C_1} + \frac{-2b}{\sqrt{\alpha}}\right] + x_1(0)$$

To obtain x_2:

Substitute the expression for x_3 in to Equation A.0.7 and by integration the following solution is found:

$$x_2 = \frac{1}{C_2}\left[\frac{k}{j\sqrt{\alpha}}e^{j\sqrt{\alpha}t} + \frac{\bar{k}}{-j\sqrt{\alpha}}e^{-j\sqrt{\alpha}t} + \frac{I_L t}{\alpha\gamma C_1} + \frac{-2b}{\sqrt{\alpha}}\right] + x_2(0)$$

To obtain x_4:

$\dot{x}_4$ is defined as from Equation A.0.1: and by integration x_4 is determined as:

$$x_4 = \frac{V_O t}{L_2} - M\left[ke^{j\sqrt{\alpha}t} + \bar{k}e^{-j\sqrt{\alpha}t} + \frac{I_L}{\alpha\gamma C_1}\right] - x_3(0) + x_4(0)$$

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Summarised solutions

$$x_1 = \frac{I_L t}{C_1} - \frac{1}{C_1}\left[\frac{k}{j\sqrt{\alpha}}e^{j\sqrt{\alpha}t} + \frac{\bar{k}}{-j\sqrt{\alpha}}e^{-j\sqrt{\alpha}t} + \frac{I_L t}{\alpha\gamma C_1} + \frac{-2b}{\sqrt{\alpha}}\right] + x_1(0)$$

$$x_2 = \frac{1}{C_2}\left[\frac{k}{j\sqrt{\alpha}}e^{j\sqrt{\alpha}t} + \frac{\bar{k}}{-j\sqrt{\alpha}}e^{-j\sqrt{\alpha}t} + \frac{I_L t}{\alpha\gamma C_1} + \frac{-2b}{\sqrt{\alpha}}\right] + x_2(0)$$

$$x_3 = ke^{j\sqrt{\alpha}t} + \bar{k}e^{-j\sqrt{\alpha}t} + \frac{I_L}{\alpha C_1 \gamma} + x_3(0)$$

$$x_4 = \frac{V_O t}{L_2} - M\left[ke^{j\sqrt{\alpha}t} + \bar{k}e^{-j\sqrt{\alpha}t} + \frac{I_L}{\alpha\gamma C_1}\right] - x_3(0) + x_4(0)$$

with the constants defined as:

$$\gamma = \left[L_1 - \frac{M^2}{L_2}\right]$$

$$\alpha = \left[\frac{1}{\gamma C_1} + \frac{1}{\gamma C_2}\right]$$

$$k = \left(\frac{1}{2}\left[x_3(0) - \frac{I_L}{\alpha\gamma C_1}\right]\right) + j\left(\frac{x_1(0) - x_2(0) + \frac{M}{L2}V_O}{2\sqrt{\alpha}\gamma}\right)$$

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A.0.3 State 2

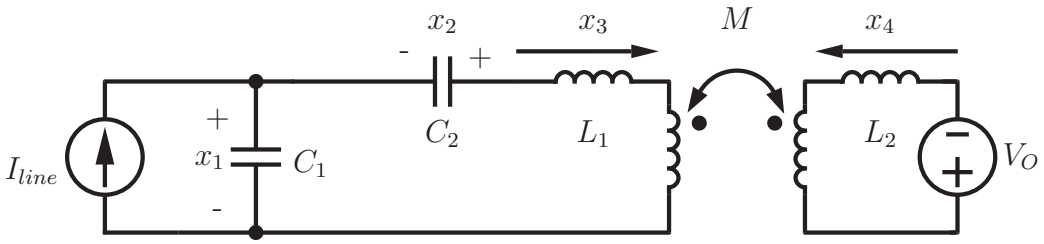

Figure A.7 – State 2 Circuit Diagram

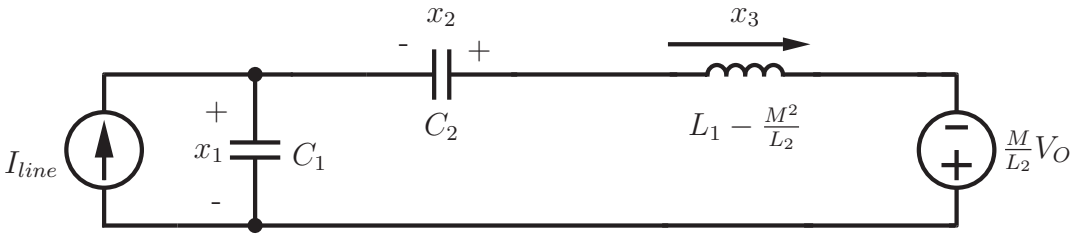

Figure A.8 – State 2 Equivalent Circuit Diagram

To obtain solutions for State 2, substitute $V_O = -V_O$ for the solutions of State 1.

Summarised solutions

$$x_1 = \frac{I_L t}{C_1} - \frac{1}{C_1}\left[\frac{k}{j\sqrt{\alpha}}e^{j\sqrt{\alpha}t} + \frac{\bar{k}}{-j\sqrt{\alpha}}e^{-j\sqrt{\alpha}t} + \frac{I_L t}{\alpha\gamma C_1} + \frac{-2b}{\sqrt{\alpha}}\right] + x_1(0)$$

$$x_2 = \frac{t}{C_2}\left[\frac{k}{j\sqrt{\alpha}}e^{j\sqrt{\alpha}t} + \frac{\bar{k}}{-j\sqrt{\alpha}}e^{-j\sqrt{\alpha}t} + \frac{I_L t}{\alpha\gamma C_1} + \frac{-2b}{\sqrt{\alpha}}\right] + x_2(0)$$

$$x_3 = ke^{j\sqrt{\alpha}t} + \bar{k}e^{-j\sqrt{\alpha}t} + \frac{I_L}{\alpha C_1\gamma} + x_3(0)$$

$$x_4 = \frac{(-V_O)t}{L_2} - M\left[ke^{j\sqrt{\alpha}t} + \bar{k}e^{-j\sqrt{\alpha}t} + \frac{I_L}{\alpha\gamma C_1}\right] + x_4(0)$$

with the constants defined as:

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$$\gamma = \left[L_1 - \frac{M^2}{L_2} \right]$$

$$\alpha = \left[\frac{1}{\gamma C_1} + \frac{1}{\gamma C_2} \right]$$

$$k = \left(\frac{1}{2} \left[x_3(0) - \frac{I_L}{\alpha \gamma C_1} \right] \right) + j \left(\frac{x_1(0) - x_2(0) + \frac{M}{L2}(-V_O)}{2\sqrt{\alpha}\gamma} \right)$$

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A.0.4 State 3

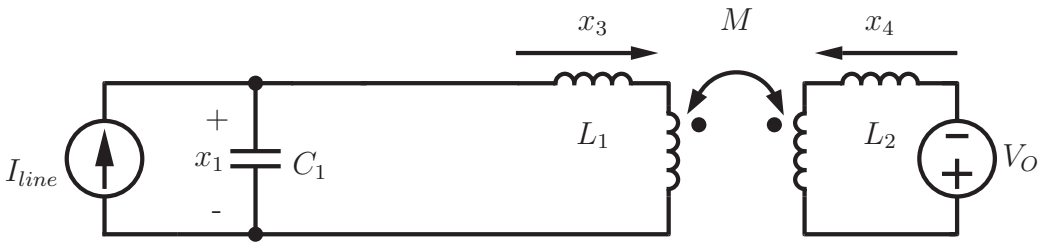

Figure A.9 – State 3 Circuit Diagram

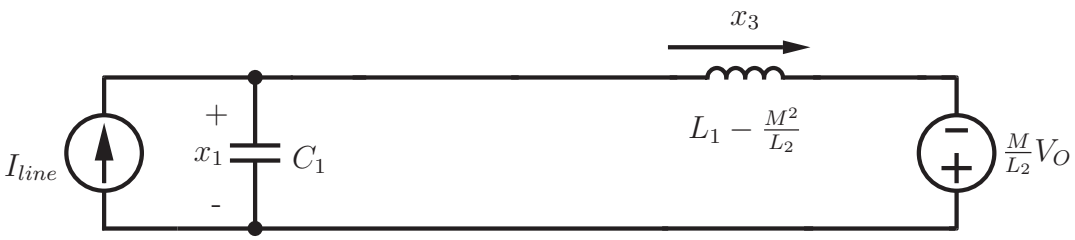

Figure A.10 – State 3 Equivalent Circuit Diagram

Equations obtained from equivalent circuit:

$$I_L = C_1\dot{x}_1 + x_3 \tag{A.0.17}$$

$$\dot{x}_2 = 0$$

$$0 = x_1 - \gamma\dot{x}_3 - \frac{M}{L_2}V_O \tag{A.0.18}$$

with

$$\gamma = \left[L_1 - \frac{M^2}{L_2}\right]$$

Rearrange Equations A.0.17 and A.0.18 to obtain:

$$\dot{x}_1 = \frac{1}{C_1}I_L - \frac{1}{C_1}x_3 \tag{A.0.19}$$

$$\dot{x}_3 = \frac{1}{\gamma}x_1 - \frac{M}{\gamma L_2}V_O \tag{A.0.20}$$

To solve x_3 and β Equation A.0.20 and the same procedure as described for state 1 one is used. The constants are found to be as follows:

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$$\alpha = \left[\frac{1}{\gamma C_1}\right]$$

$$k = \left(\frac{1}{2}\left[x_3(0) - \frac{I_L}{\alpha\gamma C_1}\right]\right) + j\left(\frac{x_1(0) + \frac{M}{L2}(-V_O)}{2\sqrt{\alpha}\gamma}\right)$$

To obtain x_1 use Equation A.0.19 and by integration the following solution is found:

$$x_1 = \frac{I_L t}{C_1} - \frac{1}{C_1}\left[\frac{k}{j\sqrt{\alpha}}e^{j\sqrt{\alpha}t} + \frac{\bar{k}}{-j\sqrt{\alpha}}e^{-j\sqrt{\alpha}t} + \frac{I_L t}{\alpha\gamma C_1} + \frac{-2b}{\sqrt{\alpha}}\right] + x_1(0)$$

To obtain x_4:
$\dot{x}_4$ is defined as from Equation A.0.1: and by integration x_4 is determined as:

$$x_4 = \frac{V_O t}{L_2} - M\left[ke^{j\sqrt{\alpha}t} + \bar{k}e^{-j\sqrt{\alpha}t} + \frac{I_L}{\alpha\gamma C_1}\right] + x_4(0)$$

Summarised solutions

$$x_1 = \frac{I_L t}{C_1} - \frac{1}{C_1}\left[\frac{k}{j\sqrt{\alpha}}e^{j\sqrt{\alpha}t} + \frac{\bar{k}}{-j\sqrt{\alpha}}e^{-j\sqrt{\alpha}t} + \frac{I_L t}{\alpha\gamma C_1} + \frac{-2b}{\sqrt{\alpha}}\right] + x_1(0)$$

$$x_2 = \frac{t}{C_2}\left[\frac{k}{j\sqrt{\alpha}}e^{j\sqrt{\alpha}t} + \frac{\bar{k}}{-j\sqrt{\alpha}}e^{-j\sqrt{\alpha}t} + \frac{I_L t}{\alpha\gamma C_1} + \frac{-2b}{\sqrt{\alpha}}\right] + x_2(0)$$

$$x_3 = ke^{j\sqrt{\alpha}t} + \bar{k}e^{-j\sqrt{\alpha}t} + \frac{I_L}{\alpha C_1\gamma} + x_3(0)$$

$$x_4 = \frac{V_O t}{L_2} - M\left[ke^{j\sqrt{\alpha}t} + \bar{k}e^{-j\sqrt{\alpha}t} + \frac{I_L}{\alpha\gamma C_1}\right] + x_4(0)$$

with the constants defined as:

$$\gamma = \left[L_1 - \frac{M^2}{L_2}\right]$$

$$\alpha = \left[\frac{1}{\gamma C_1} + \frac{1}{\gamma C_2}\right]$$

$$k = \left(\frac{1}{2}\left[x_3(0) - \frac{I_L}{\alpha\gamma C_1}\right]\right) + j\left(\frac{x_1(0) - x_2(0) + \frac{M}{L2}V_O}{2\sqrt{\alpha}\gamma}\right)$$

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A.0.5 State 4

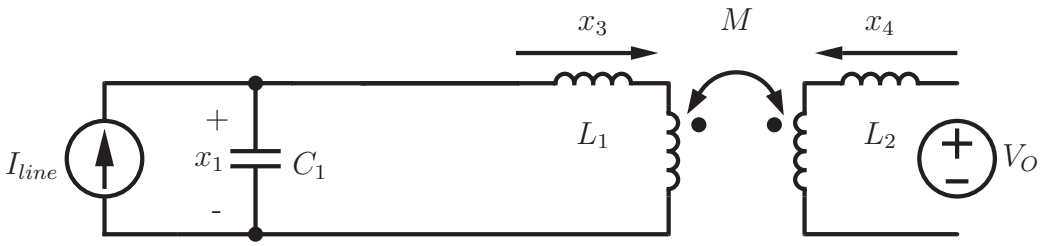

Figure A.11 – State 4 Circuit Diagram

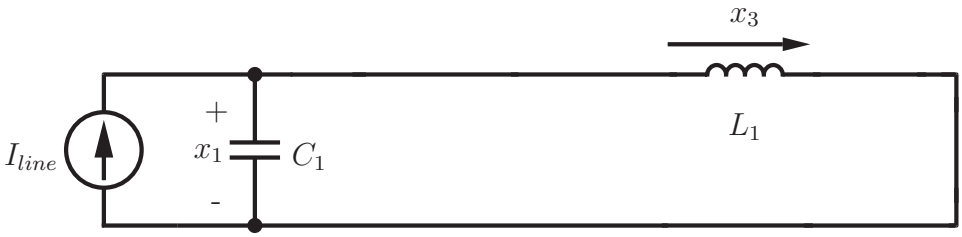

Figure A.12 – State 4 Equivalent Circuit Diagram

Equations obtained from equivalent circuit:

$$I_L = C_1\dot{x}_1 + x_3 \tag{A.0.21}$$

$$\dot{x}_2 = 0$$

$$\dot{x}_3 = \frac{1}{\gamma}x_1 \tag{A.0.22}$$

$$\dot{x}_4 = 0$$

with

$$\gamma = L_1$$

Rearrange Equations A.0.21 and A.0.22 to obtain:

$$\dot{x}_1 = \frac{1}{C_1}I_L - \frac{1}{C_1}x_3 \tag{A.0.23}$$

$$\dot{x}_3 = \frac{1}{L_1}x_1 \tag{A.0.24}$$

To solve x_3 and β, the same procedure as described for state 1 one is applied to Equation A.0.24. The constants are found to be as follows:

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$$\alpha = \left[\frac{1}{\gamma C_1}\right]$$

$$k = \left(\frac{1}{2}\left[x_3(0) - \frac{I_L}{\alpha\gamma C_1}\right]\right) + j\left(\frac{-x_1(0)}{2\sqrt{\alpha}\gamma}\right)$$

To obtain x_1, use Equation A.0.23 and by integration the following solution is found:

$$x_1 = \frac{I_L t}{C_1} - \frac{1}{C_1}\left[\frac{k}{j\sqrt{\alpha}}e^{j\sqrt{\alpha}t} + \frac{\bar{k}}{-j\sqrt{\alpha}}e^{-j\sqrt{\alpha}t} + \frac{I_L t}{\alpha\gamma C_1} + \frac{-2b}{\sqrt{\alpha}}\right] + x_1(0)$$

Summarised solutions

$$x_1 = \frac{I_L t}{C_1} - \frac{1}{C_1}\left[\frac{k}{j\sqrt{\alpha}}e^{j\sqrt{\alpha}t} + \frac{\bar{k}}{-j\sqrt{\alpha}}e^{-j\sqrt{\alpha}t} + \frac{I_L t}{\alpha\gamma C_1} + \frac{-2b}{\sqrt{\alpha}}\right] + x_1(0)$$

$$x_2 = 0$$

$$x_3 = ke^{j\sqrt{\alpha}t} + \bar{k}e^{-j\sqrt{\alpha}t} + \frac{I_L}{\alpha\gamma C_1}$$

$$x_4 = 0$$

with the constants defined as:

$$\gamma = L_1$$

$$\alpha = \left[\frac{1}{\gamma C_1}\right]$$

$$k = \left(\frac{1}{2}\left[x_3(0) - \frac{I_L}{\alpha\gamma C_1}\right]\right) + j\left(\frac{-x_1(0)}{2\sqrt{\alpha}\gamma}\right)$$

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A.0.6 State 5

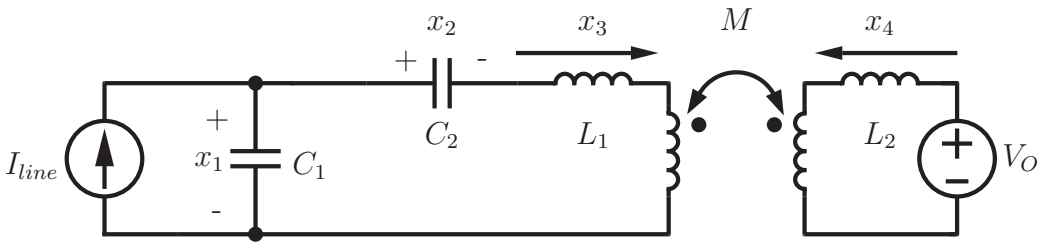

Figure A.13 – State 5 Circuit Diagram

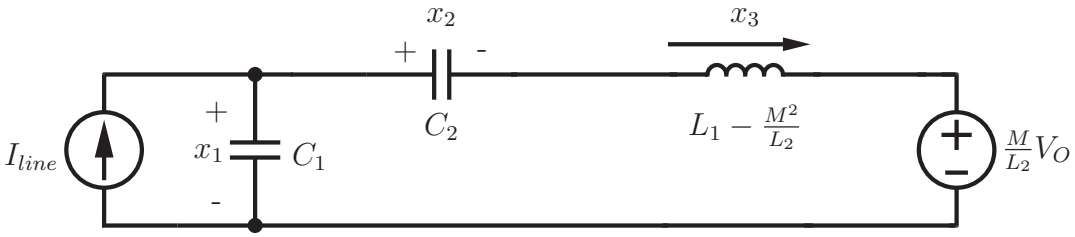

Figure A.14 – State 5 Equivalent Circuit Diagram

To obtain solutions for state 5, substitute $x_2 = -x_2$ and $\dot{x}_2 = -\dot{x}_2$ for the solutions of State 1.

Summarised solutions

$$x_1 = \frac{I_{line}t}{C_1} - \frac{1}{C_1}\left[\frac{k}{j\sqrt{\alpha}}e^{j\sqrt{\alpha}t} + \frac{\bar{k}}{-j\sqrt{\alpha}}e^{-j\sqrt{\alpha}t} + \frac{I_{line}t}{\alpha\gamma C_1} + \frac{-2b}{\sqrt{\alpha}}\right] + x_1(0)$$

$$x_2 = -\left[\frac{t}{C_2}\left[\frac{k}{j\sqrt{\alpha}}e^{j\sqrt{\alpha}t} + \frac{\bar{k}}{-j\sqrt{\alpha}}e^{-j\sqrt{\alpha}t} + \frac{I_{line}t}{\alpha\gamma C_1} + \frac{-2b}{\sqrt{\alpha}}\right] + x_2(0)\right]$$

$$x_3 = ke^{j\sqrt{\alpha}t} + \bar{k}e^{-j\sqrt{\alpha}t} + \frac{I_{line}}{\alpha C_1\gamma} + x_3(0)$$

$$x_4 = \frac{V_O t}{L_2} - M\left[ke^{j\sqrt{\alpha}t} + \bar{k}e^{-j\sqrt{\alpha}t} + \frac{I_{line}}{\alpha\gamma C_1}\right] + x_4(0)$$

with the constants defined as:

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$$\gamma = \left[L_1 - \frac{M^2}{L_2} \right]$$

$$\alpha = \left[\frac{1}{\gamma C_1} + \frac{1}{\gamma C_2} \right]$$

$$k = \left(\frac{1}{2} \left[x_3(0) - \frac{I_{line}}{\alpha \gamma C_1} \right] \right) + j \left(\frac{x_1(0) - x_2(0) + \frac{M}{L2} V_O}{2\sqrt{\alpha}\gamma} \right)$$

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A.0.7 State 6

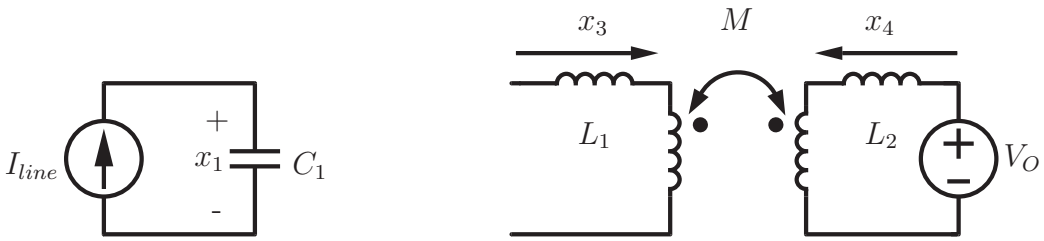

Figure A.15 – State 6 Circuit Diagram

To obtain x_1:

$$I_{line} = C_1 \dot{x}_1$$
$$\dot{x}_1 = \frac{I_{line}}{C_1} \tag{A.0.25}$$

Integrate Equation A.0.25 with $x_1(0)$ as initial condition

$$x_1 = \frac{I_{line}}{C_1} t + x_1(0)$$

To obtain x_2 with $x_2(0)$ as the initial condition:

$$x_2 = x_2(0)$$

To obtain x_3:
From simulation

$$x_3 = 0$$

To obtain x_4
From Equation A.0.7

$$\dot{x}_3 = 0$$

From circuit diagram

$$V_O = L_2 \dot{x}_4$$
$$\dot{x}_4 = \frac{V_O}{L_2} \tag{A.0.26}$$

Integrate Equation A.0.26

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$$x_4 = \frac{V_O}{L_2}t + x_4(0)$$

with $x_4(0)$ as the initial condition.

Summarised solutions

$$\begin{aligned} x_1 &= \frac{I_{line}}{C_1}t + x_1(0) \\ x_2 &= x_2(0) \\ x_3 &= 0 \\ x_4 &= \frac{V_O}{L_2}t + x_4(0) \end{aligned}$$

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